

New Efficient Algorithm for Mapping Linear Array into Hex-Cell Network

Mohammad Qatawneh

*Department of Computer Science, KASIT, University of Jordan,
P.O. Box 13047, Amman11942, Jordan
mohd.qat@ju.edu.jo*

Abstract

This paper introduces a new efficient algorithm for mapping linear array into hex-cell network. The capability of mapping several topologies is considered as one of the most important features of the hex-cell interconnection network. This feature is strongly affecting the performance of parallel machines. In this paper, we present a new algorithm for mapping linear array topology into hex-cell network with dilation and congestion of one; which indicates that we have one-to-one mapping as a result of intercommunication among nodes.

Keywords: Mapping, Hex-Cell network, Linear Array, Dilation, Congestion

1. Introduction

The choice of using interconnection network topology is considered as one of the most important issues that must be taken into consideration when designing and implementing parallel systems as well as when developing distributed applications. Therefore, several interconnection network topologies such as tree, mesh, hypercube, tree-hypercubes, bus, ring, and hex-cell have been proposed for this reason [1-4]. Each network topology has its own features such as: node degree, network degree, diameter, bisection bandwidth, routing algorithm, partitioning, mapping and so on. Those features greatly affect the performance of parallel and distributed systems. One of the critical properties of any interconnection network that received more attention is the study of mapping issue.

The mapping issue is a technique that maps a source graph (interconnection network topology) $G_s = (V_s, E_s)$ into another target graph $G_t = (V_t, E_t)$. The process of mapping graph G_s into graph G_t involves mapping each vertex in the set V_s into vertex or a set of vertices in set V_t and each edge in the set E into an edge or a set of edges in E_t . When mapping graph $G_s = (V_s, E_s)$ into another target graph $G_t = (V_t, E_t)$, the following three parameters are important to evaluate mapping result.

The first one is criterion, dilation, which is the maximum number of links in target graph G_t , that any edge in source graph G_s is mapped into. The second is congestion, which is the maximum number of edges mapped into any edge in V_t . The congestion is the key factor affecting the system delay and packet loss during data transmission. Third, the sets V_s and V_t may contain different numbers of vertices. In this case, a node in V_s corresponds to more than one node in V_t . The ratio of the number of nodes in the set V_t to that in set V_s is called the expansion of the mapping.

The ability of mapping several networks into hex-cell, symmetry, regularity, strong resilience, and simple routing have made hex-cell network superior to many other multicomputer networks [1]. In this paper, we propose a new efficient algorithm for mapping linear array into Hex-Cell interconnection network.

The rest of this paper is organized as follows. In Section 2, we present the definition of hex-cell interconnection network. Section 3 presents the new addressing scheme for Hex-Cell and the proposed mapping algorithm. Section 4 summarize and conclude the paper.

2. Definition of Hex-Cell Network

A Hex-Cell network with depth d is denoted by $HC(d)$ and can be constructed by using units of hexagon cells, each of six nodes [1]. A Hex-Cell network with depth d has d levels numbered from 1 to d , where, level 1 represents the innermost level corresponding to one hexagon cell. Level 2 corresponds to the six hexagon cells surrounding the hexagon at level 1. Level 3 corresponds to the 12 hexagon cells surrounding the six hexagons at level 2 as shown in figure 1. The levels of the $HC(d)$ network are labeled from 1 to d . Each level i has N_i nodes, representing processing elements and interconnected in a ring structure. Figure 2 shows the addressing nodes in HC.

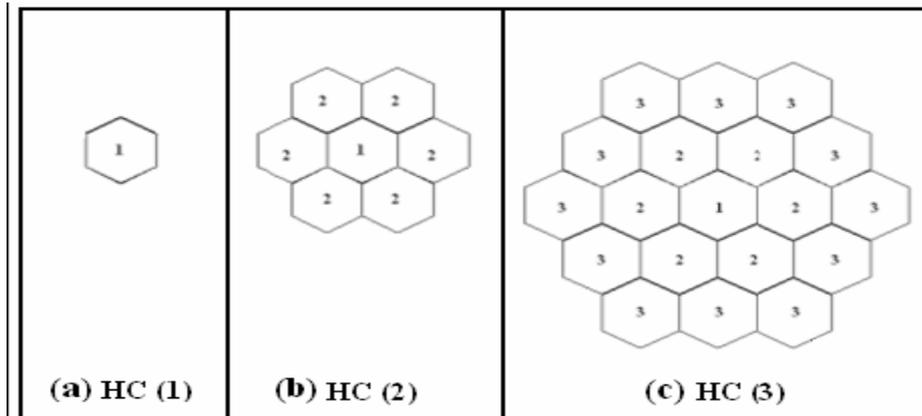


Figure 1. (a) HC (One Level) (b) HC (Two Levels) (c) HC (Three Levels)

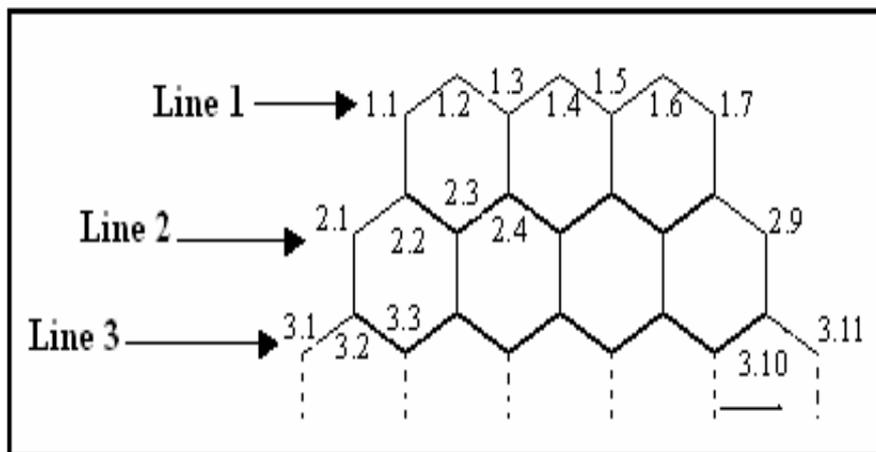


Figure 2. Addressing Nodes in HC [1]

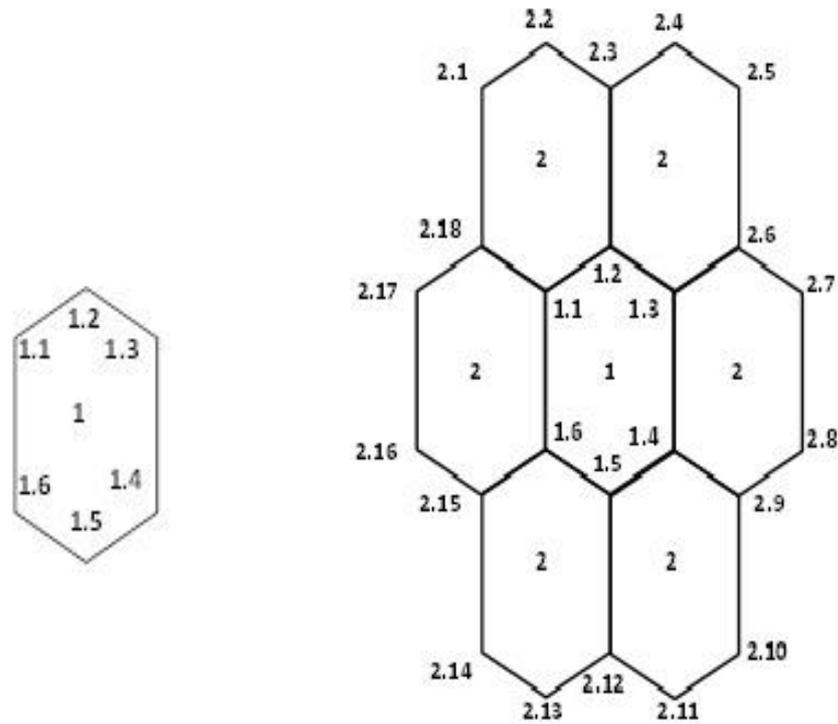
3. Proposed Mapping Algorithm

In this section, we present the new addressing scheme for Hex-Cell network, the proposed mapping Algorithm, and a discussion via an example.

3.1. The New Addressing Scheme for Hex-Cell Network

This section presents a new addressing scheme for Hex-Cell network. The levels of a network with depth d are numbered as labeled from 1 for the innermost level to d for the outermost level. Each node in hex-cell is identified by a pair (X, Y) , where X denotes the level number, and Y denotes the location of the node in that level as shown in Figure 3 and 4. A node with address $(3, 1)$ is the first node that exists at the level number 3.

Address (3.2) refers to the second node that exists at the level number 3, and so on till we reach to the last node in that level, notice that we circling with clock direction. The same approach is applied for all levels till we reach the innermost level.



a) HC(1)

b) HC(2)

Figure 3. New Addressing Scheme for Hex-Cell Network

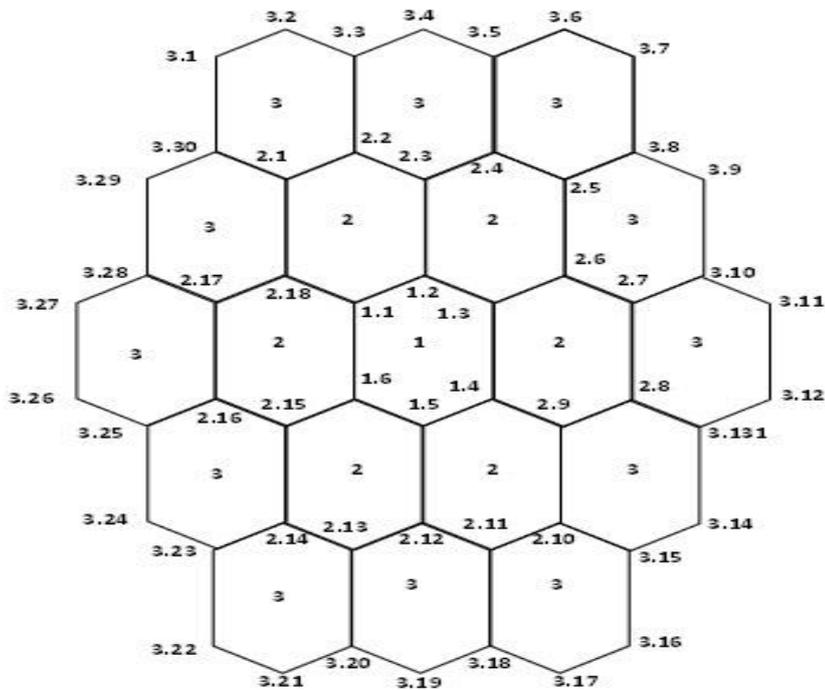


Figure 4. New Addressing Scheme for Hex-Cell Network HC(3)

3.2. The Proposed Mapping Algorithm

In this section, we present a new algorithm for mapping linear array network into hex-cell network. Based on the above addressing scheme, the proposed mapping algorithm is designed as shown in Figure 4.

Step 1: The first node located in the outer level is considered as the start point.

Step 2: Add the address of the start node to Node-Queue and mark it as checked node.

Where X denotes the level number, d the network depth, and Y the location of the node in that level.

Step 3: For X = d to 1
 For Y=1 to 6(2d -1)
 Next node = (X,Y)
 Y++
 X --

Step 4: End.

Figure 5. Proposed Mapping Algorithm

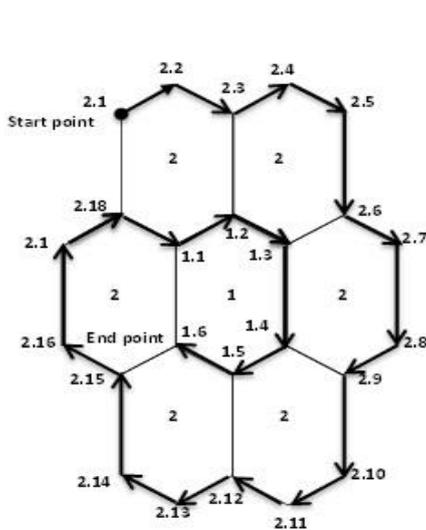


Figure 6. Mapping Linear Array in TH(2)

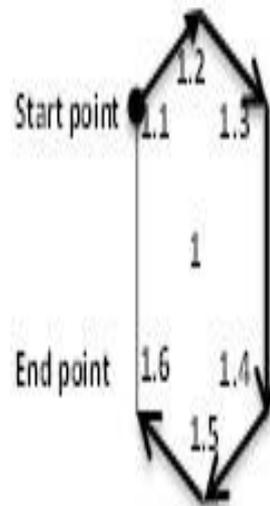


Figure 7. Mapping Linear Array in TH(1)

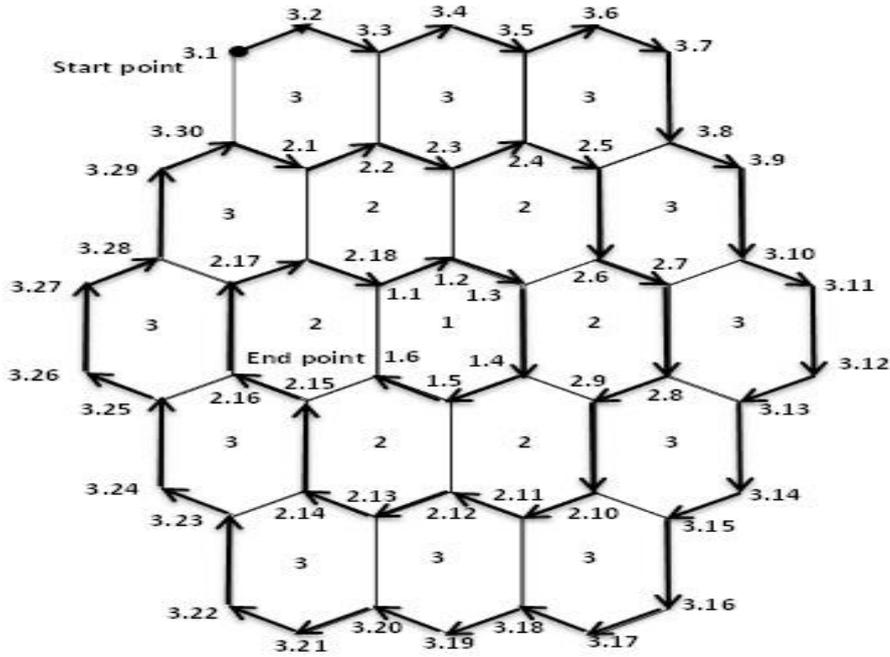


Figure 8. Mapping Linear Array in TH(3)

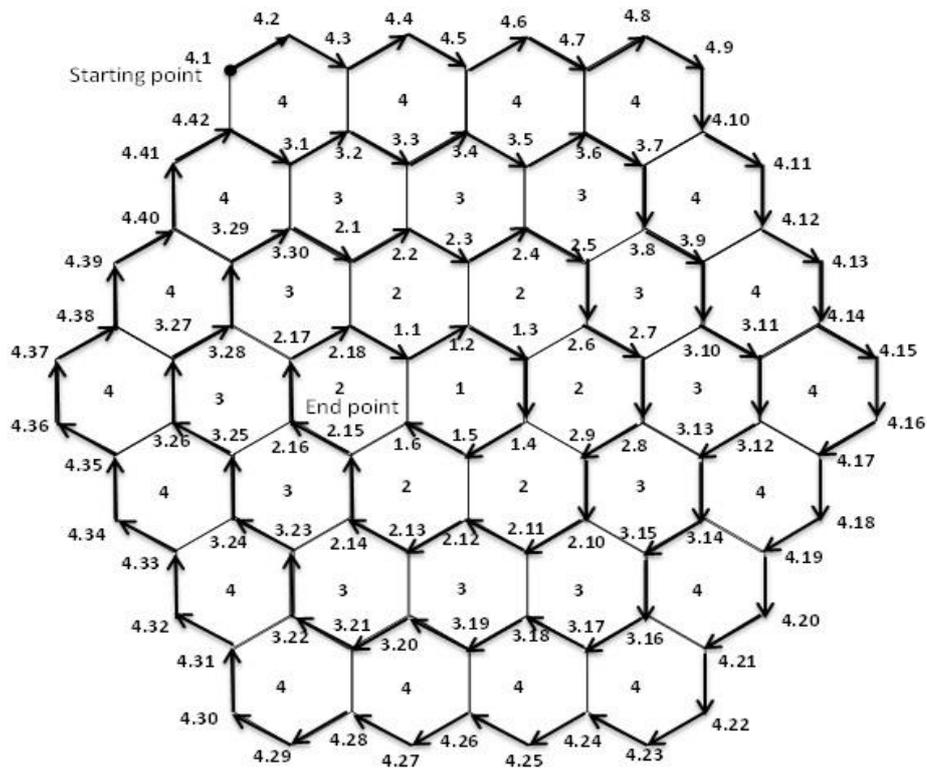


Figure 9. Mapping Linear Array in T4(2)

3.3. Discussions via Example

The following example explains the mapping of linear array into hex-cell network. For this purpose, we consider a network of a Hex-cell topology with 3 levels; *i.e.*, HC(3) as shown in Figure 8. When applying the proposed mapping algorithm in Figure 5, the start

node will be (3,1) where (X=3, and Y=1). By executing the steps 2 and then step 3 for the first iteration, it reaches to the node (3,30) in level 3. In step 3 outer loop's second iteration (X=2, and Y=1), it starts at the node (2,1) and iterates until it reaches node (2,18). In step 3 outer loop's third iteration (X=1, and Y=1), it starts at the node (1,1) and iterates until it reaches node (1,6) (see: Figure 8).

4. Conclusion

In this paper, we proposed and evaluated a new addressing scheme and an efficient algorithm for mapping linear array into hex-cell interconnection network. The new addressing scheme deals with levels and node numbers which overcome the limitations of the addressing mode proposed in [1] in terms of no need to readdressing the topology when adding new levels. The Evaluation results show that the congestion, dilation and expansion are equal to 1.

Acknowledgment

This work was supported by the University of Jordan for my sabbatical leave year 2015 – 2016.

References

- [1] S. Ahmad, M. Qatawneh, A. Wesam and S. Azzam, "Hex-Cell: Modeling, Topological Properties and Routing Algorithm", *European Journal of Scientific Research*, vol. 22, no. 2, (2008), pp. 457-468.
- [2] Q. Mohammad, A. Alamoush, S. Basem, M. M. Al Assaf and M. Sh. Daoud, "Embedding Bus and Ring into Hex-Cell Interconnection Network", *International Journal of Computer networks and communications*, vol. 7, no. 3, (2015).
- [3] M. Qatawneh, A. Alamoush and J. Alqatawna, "Section Based Hex-Cell Routing Algorithm (SBHCR)", *International Journal of Computer Networks and Communications*, vol. 7, no. 1, (2015).
- [4] Q. Mohammad and H. Khattab, "New Routing for Hex-Cell Network", *International Journal of Future Generation Communication and Networking*, vol. 8, no. 2, (2015).
- [5] W. Almobaideen, M. Qatawneh, A. Sleit, I. Salah and S. Al-Sharaeh, "Efficient mapping scheme of ring topology onto tree-hypercubes", *Journal of Applied Sci.*, vol. 7, (2007), pp. 2666-2670.
- [6] M. Qatawneh, "Embedding linear array onto tree-hypercube network", *European Journal of scientific Research*, vol. 10, no. 2, (2005), pp. 72-76.
- [7] C. Decayeux and D. Seme, "3D hexagonal network: modeling, topological properties, addressing scheme, and optimal routing algorithm", *IEEE Transactions on Parallel and Systems*, vol. 16, no. 9, (2005).
- [8] J. Baril and V. Vajnovzki, "Minimal change list for Lucas strings and some graph theoretic consequences", *Elsevier. Theoretical Computer Science*, vol. 346, (2005), pp. 189-199.
- [9] A. Ernastuti and V. Vajnovzki, "Embeddings of linear arrays, Rings and 2-d dimensions on extended Lucas cube networks", *Proceedings of the International Conference on Electrical Engineering and Informatics Institute Teknologi Bandung, Indonesia*, (2007), pp. 17-19.
- [10] M. Yang, J. Jimmy and L. Hsu, "Hamiltonian circuit and linear array embeddings in faulty k-ary-n-cubes", *Journal of Parallel Distrib. Comput.*, vol. 67, (2007), pp. 362-368.

Author



Prof. Mohammad Qatawneh, is the dean of the King Abdullah II School for Information Technology (KASIT) at the University of Jordan. He received his Ph.D. in computer from Kiev University in 1996. Prof. Qatawneh published thirty papers in the areas of Networks, Parallel algorithms and Embedding systems. His research interests include Parallel Computing, Interconnection Networks and Routing Algorithms.