International Journal of Advanced Science and Technology
Vol.90 (2016), pp.1-8
http://dx.doi.org/10.14257/ijast.2016.90.01

Temperature Aware Methodology for Low Power SoC System

Suresh Kumar. K[1], Anitha S.[2] and Gayathiri M.[3]

[1]*PG Scholar, Knowledge Institute of Technology, Salem, India*
[2]*Assistant Professor, Knowledge Institute of Technology, Salem, India*
[3]*Assistant Professor, Knowledge Institute of Technology, Salem, India*

Abstract

Energy consumption is a major concern in many embedded computing systems. Several studies have shown that cache memories account for about 50% of the total energy consumed in these systems. The performance of a given cache architecture is determined to a large degree by the behavior of the application executing on the architecture. The Desktop systems have to accommodate a very wide range of applications and therefore the cache architecture is usually set by the manufacturer as a best compromise given current applications, technology and cost. Unlike desktop systems, embedded systems are designed to run a small range of well-defined applications. In this paper, we explore the tradeoff between thermal and interconnect energy when allocating tasks in MPSoC and to devlop an efficient system. The experimental results show that the devloped technique can reduce interconnects energy by more than 25% on an average with almost the same peak temperature when compared with prior thermal-balanced solutions.

Key words: *TSV, DCR, Interconnect energy, Cache Management*

1. Introduction

Three-dimensional integrated circuits (3-D ICs), where two or more layers of active electronic components are integrated vertically into a single chip, significantly reduces the on chip wire length that often becomes a major bottleneck of performance and/or power dissipation in 2-D ICs. Particularly, 3-D memory stacking has received a great attention since it resolves the memory bandwidth challenges of 2-D ICs by stacking cache memory onto a multi-core die. However, the high power density resulting from multiple (memory) die stacking may lead to the temperature-related problems in reliability, power, performance and cooling cost. Especially the exponential dependence of leakage power on temperature in conjunction with the large amount of cache stacked onto a multi-core die might aggravate the energy efficiency of 3-D processor-memory systems, when considering that on-chip SRAM cache often consumes almost half of total energy in a microprocessor system.

Dynamic cache reconfiguration (DCR) is an effective method to reduce cache energy by configuring capacity, line size and associatively of cache according to work load characteristics and turning off unused parts of the cache. For example the amount of turned on cache blocks can be optimally determined and assigned to each core based on the memory access demands of applications and then the unassigned cache blocks can be turned off to reduce the operating temperature and the temperature induced leakage energy. However, excessive power gating of cache blocks may incur performance degradation due to the increase in cache misses.

Each core has a low-latency and large bandwidth access to the cache banks directly stacked on it (*i.e.*, local cache banks) through-silicon vias (TSVs). The core is also able to access cache banks stacked on the other cores (*i.e.*, remote cache banks), but the corresponding memory transaction has to be done through the cross bar switch with longer latency. Since cache banks directly stacked on a core share the same TSVs, traffic

ISSN: 2005-4238 IJAST

collision might occur even when cores access different cache banks if the cache banks are directly stacked on the same core (and share the same TSVs).

In this paper, we devlop a dynamic cache reconfiguration (DCR) scheme that minimizes the energy consumption of 3-D CMPs with temperature and time-to-deadline constraints. Given the time varying temperature profile of cores and L2 cache banks, the devloped solution determines the number of L2 cache banks (*i.e.*, the amount of cache capacity) logically allocated to each core and the physical placement of the allocated L2 cache banks considering both temperature distribution and memory traffic of the 3-D CMPs. To the best of our knowledge, this is the first work on online DCR schemes for real-time 3-D CMPs that considers both temperature and memory traffic. Considering both temperature distribution and cache traffic congestion gives more energy reduction than considering only one without the other. A key challenge in 3D memory stacking is the heat generated from the 3D chip with its increased power density. In case of memory-stacked CMP systems, temperature of each core directly affects the temperature of cache memory blocks stacked on the core. There are prior works on the temperature aware management for 3D CMP. Since work load characteristics such as memory access behavior change dramatically at runtime, online adaptive configuration of cache memory is paramount for energy reduction. We also investigate the impact of non-uniform cache access latency, cache traffic congestion and temperature distribution on the energy consumption of 3- D CMPs.

2. Related Work

A number of studies have investigated the challenges of stacked-die architectures and have attempted to address the need for an analysis and exploration methodology for 3-D designs. MEVA3-D is one such exploration tool that enables automated floor planning, routing, placement of TSVs and the thermal profiling of stacked-die architectures. A demonstration of the tool applied to the 3-D design of a conventional processor core illustrated the performance benefits of stacked-die architectures and their associated thermal issues. However, this paper does not describe the planning of the 3-D TSV network, nor the KOZ considerations considered in their placement. In addition, while MEVA3-D includes support for thermal via insertion, it does not support the use of a runtime power management alongside the performance simulation. The conceptual idea of the simulation of a two-tier stack with a vertical interconnects. Here, functional blocks on two tiers communicate through a vertical interconnect. This comprises of interfacing adapters and parameterized driver-to-load (D to L) vertical path models. We do not perform a functional simulation of blocks during TSV topology exploration, but only an electrical simulation using the vertical path model. The D to L path model is instantiated multiple times to simulate several TSV topologies simultaneously.

3. Problem Statement

While 3-D integration is seen as a promising solution toward sustaining the trend of increasing integration densities, a number of challenges arise from the stacking of silicon dies. Two such critical issues include the KOZ, necessitated by mechanical stress considerations of TSVs and the consequent thermal implications of integrating multiple layers of logic in die-stacks with different vertical interconnect topologies. The problem is to find the number of cache banks allocated to each core and the physical positions of the allocated cache banks at runtime such that the overall system energy consumption while all the deadline constraints are met and the operating temperature does not exceed the maximum limit. The layer closest to the heat sink consists of multiple cores with its own private L1 cache. Multiple layers of L2 cache, each of which consists of multiple SRAM cache banks are stacked on the multi-core layer. Each cache bank has the same area or shape as that of a core. In the view of a core, local cache banks can be directly accessed,

while remote cache banks (*i.e.*, cache banks stacked on the other cores) can be accessed through the cross bar switch.

4. Power Management Scheme

The temperature constrained power management scheme for 3-D MPSoCs is implemented within the customizable power management block (PMB) which is responsible for controlling the voltage and frequency of PEs within the temperature power simulation. Figure 1 shows the conceptual control loop for the PMB. The block reads the utilization or activity rate of each PE and its temperature and the total chip power computed through a power measurement circuit within the power supply to set a new voltage and frequency levels for PEs at regular intervals.

For such a scheme to be effective, it is important to model the dynamics of the controlled system, *i.e.*, establish the relationship between the manipulated and the controlled variables. In this case, the operating voltage frequency level is used as a manipulated variable to control power and temperature of the system

Initial Updates: At the beginning of a new control period, the difference between the total chip power and the local power budget value is computed. In the event that a new temperature check cycle has started, the difference between the actual and the critical temperatures of each PE is updated.

Thermal Run out: This step ensures that the temperature of each PE is maintained within the safety margin.

Convergence Check: To prevent frequent fluctuations in the voltage-frequency levels, the algorithm considers the power value as converged when the total chip power is between 98% and 100% of the power budget value. If this is not the case, voltage-frequency levels may be scaled in the pull up or pull down stage of the algorithm. The power value is considered as converged if total chip power is between 98% and 100% of power budget value. If this is not the case, V-F levels are scaled in the next stage of the algorithm–pull up or pull down.

Pull Up or Pull Down: In this stage, the voltage-frequency level of PEs is pulled up or down based on their allocated power budget using weighted equation.

Write-Back and Reset: Finally, the voltage-frequency level determined for each PE is actuated along with the ON/OFF state signals if required. At this stage, internal parameters are reset and the algorithm is suspended until the next control cycle.

5. Circuit Selection and Fault Detection

The circuit to be tested will be selected in this phase. The circuit will be combinational or sequential circuits with number of signal lines for example c17, s27, c432, c499, c1355, c1908. The alphabet ‘c’and‘s’ denotes combinational and sequential circuits. The number behind the letter denotes number of signal lines in that circuit. Initially the circuit is tested to check whether it contains faults. In order to check we can use conventional stuck-at fault-based test pattern. They are truth table and fault matrix method, path sensitization method, D-algorithm, PODEM method.

In path sensitization method each and every path or interconnection in the circuit will be sensitized. The test vector could be found. Then the output for the test vector will be compared with fault free circuit output. The basic principle of the path sensitization method is to choose some path from the origin of the fault to the circuit output. As mentioned earlier, a path is sensitized if the inputs to the gates along the path are assigned values such that the effect of the fault can be propagated to the output. The process of

propagating the effect of the fault from its original location to the circuit output is known as the forward trace. The next phase of the method is the backward trace in which the necessary signal values at the gate outputs specified in the forward trace phase are established.

6. Test Under Multiple Voltages

In order to improve fault coverage, multiple supply voltages are applied to the circuit to be tested. Here three VDD values are taken. They are low voltage, high voltage, medium voltage (VDD low, VDD high, VDD medium). Low voltage is the threshold voltage of the circuit and medium voltage will be twice of threshold voltage and high voltage will be the maximum voltage that can be tolerated by the circuit.

For the combinational and sequential circuits the threshold voltage will be in the range of 0.8v. So the fault detectability is evaluated at three *V*DD values (*V*DDL = 0.8V, *V*DDM = 1.0 V, and *V*DDH = 1.2 V). The *V*DD values were selected to be in the range of 2 × *Vt*to the nominal *V*DD. The delay behavior for these three VDD will be different. All the three VDD will be given to each and every intervals separately. The delay behavior will vary according to the supply voltage. The fault detection threshold value can vary with supply voltages. That is, the detection thresholds at VDDL, VDDM, and VDDH respectively for gross delay faults.

The SoC fault list that is an input to the algorithm can be generated exhaustively for comprehensive fault coverage or selectively using layout-aware methodology for realistic fault locations. If the Net list corresponds to a multi voltage design, its operating *V*DD levels are used in this algorithm. However, for a multi voltage design with a large number of *V*DD levels, it is devloped that only three *V*DD levels are used (the highest, middle and lowest).

Delay Behavior

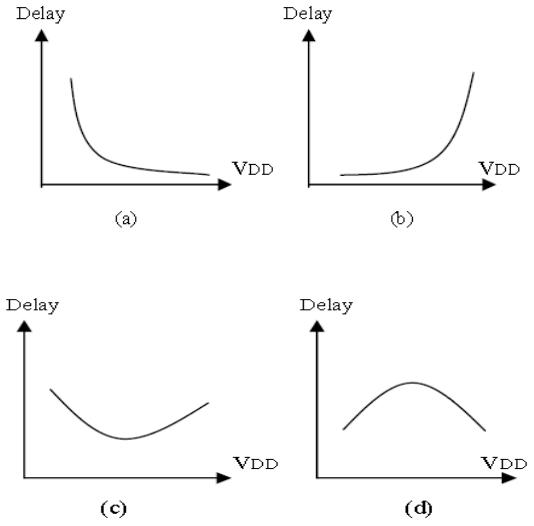

Figure 1. Behaviours Considered in the Proposed Model. (a) Decreasing Delay Behavior. (b) Increasing Delay Behavior. (c) Mid-bump Delay Behavior. (d) Mid-bump-inverter Delay Behavior

The behaviour of the delay caused by SoC fault will be observed in this phase. As in the conventional model there are four SoC delay behavior with respect to supply voltage. They are (i) Decreasing delay behaviour that is the delay will be decreased with increasing VDD.(ii) Increasing delay behavior that is the delay will be increased with

increasing VDD.(iii) Mid-bump delay behavior that is the delay will be decreased at particular voltage again it increased. (iv) Mid-bump-inv delay behaviour that is the delay will be increased at particular voltage again it decreased. In decreasing delay behavior the behavior of delay maximum at *V*DDL and minimum at *V*DDH, in increasing delay behavior maximum at *V*DDH and minimum *V*DDL, in mid-bump delay behavior minimum at *V*DDM, in mid-bump-inv delay behavior maximum at *V*DDM.

Table I. Voltage Frequency Level Transitions with the Conventional 2-D and the New 3-D Approach

		Per core		Island	
		2D	New 3D	2D	New 3D
Tier 3	*PE 11*	1	5	16	23
	PE 10	1	6	18	5
	PE 9	1	6	19	5
	PE 8	1	7	22	11
Tier 2	*PE 7*	16	4	17	23
	PE 6	12	5	20	5
	PE 5	12	5	19	5
	PE 4	11	6	25	13
Tier 1	*PE 3*	33	6	29	33
	PE 2	31	7	28	9
	PE 1	31	5	26	9
	PE 0	33	7	31	17
Aggregate freq.		67	30	111	57

7. Simulation and Synthesis Results

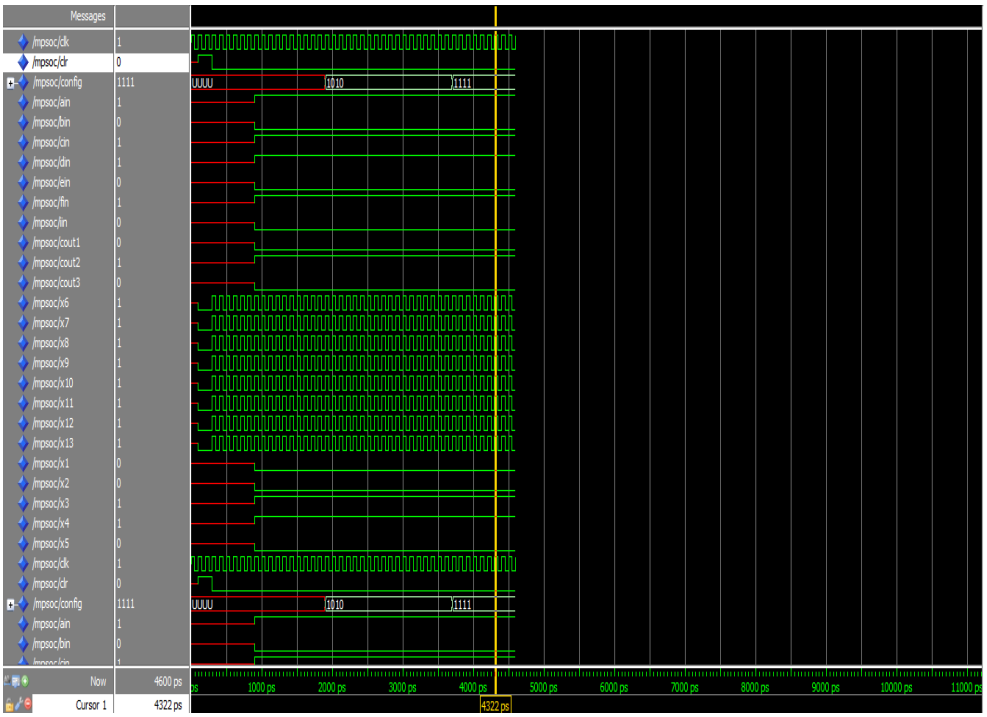

Figure 2. Simulation Results for System-on-Chip module

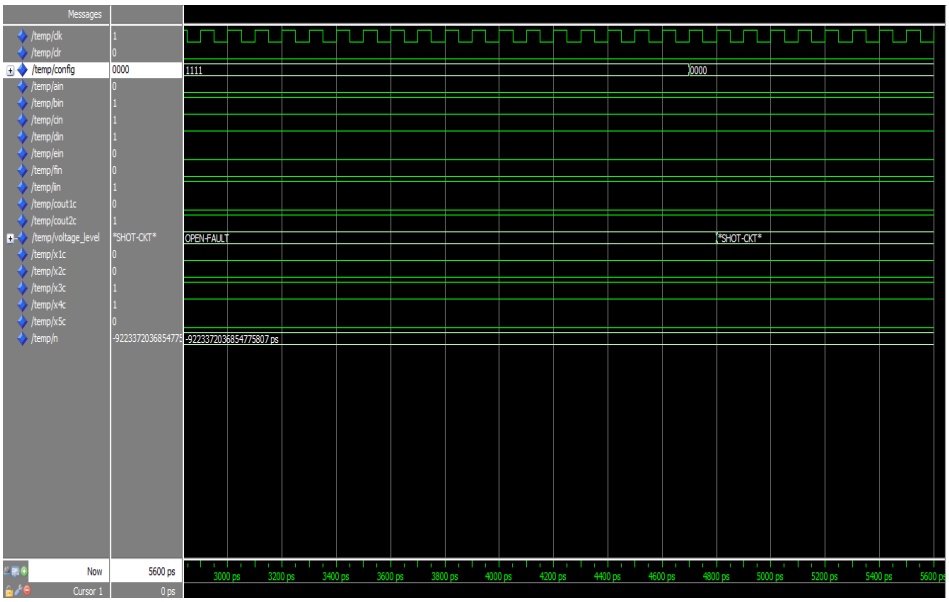

Figure 3. Simulation Results for Temperature Module

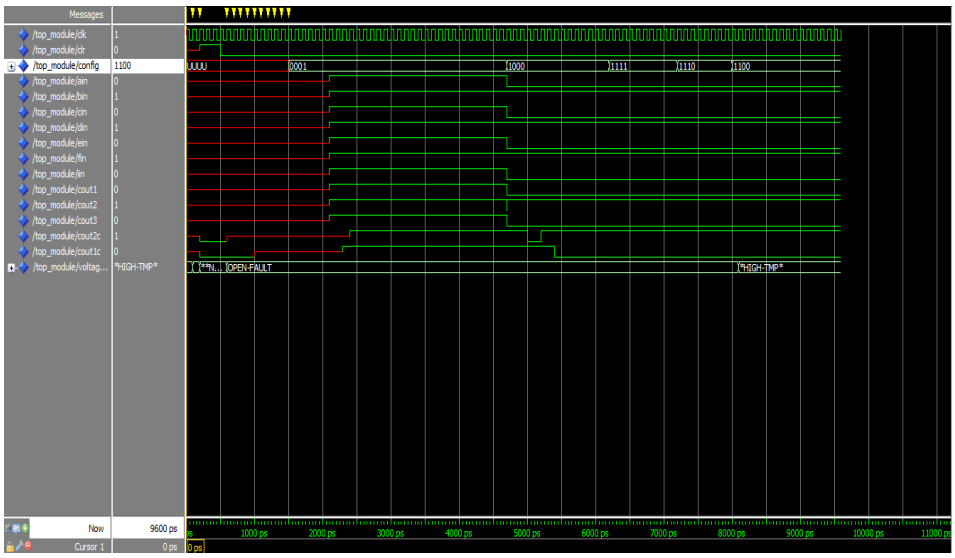

Figure 4. Simulation Results for Top Module

8. Conclusion

In this paper, we devloped a new power management mechanism for MpSoCs. The proposed fault detection mechanisms allow the accurate localization of permanent faulty routing blocks in the SoC. The effect of supply voltages on fault behaviour and detectability can be explained by this model. Differentiating temperature faults must be clearly presented. The behaviour of delay caused by SoC will be analyzed as a function of set of supply voltages. Simulation will show that the detectability and delay behavior is a function of temperature value and supply voltages. In this model the temperature range will be treated as set of continuous intervals and three detection ranges. Each interval represents different fault behavior with respect to supply voltages. Using the model, it will be shown that the observability of SoC delays that increase with VDD. The model parameter that is fault threshold will be calculated.

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