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Analysis of Three Phase Reduced Switch Nine Level Inverter with Various PWM Strategies

C. R. Balamurugan[1], S. P. Natarajan[2], R. Bensraj[3] and B. Shanthi[4]

[1]*Department of EEE, Arunai Engineering College, Tiruvannamalai*
[2,3,4]*Faculty of Engineering, Annamalai university, Chidambarama*
crbalain2010@gmail.com

Abstract

This paper proposes a three phase nine level inverter with various three phase star (Y) connected loads of R (Resistive) load, RL (Resistive Inductive) load and IM (Induction Motor) load. The various PWM (Pulse Width Modulation) control techniques were proposed. Motor load provides rated speed N (rpm) and its corresponding electromagnetic torque T (N-m). Pulse Disposition (PD) technique provides better Total Harmonic Distortion (THD) and rated speed for this proposed topology. Performance factors are like V_{RMS}, V_{PEAK}, I_{RMS}, I_{PEAK} (fundamental), THD were obtained and its FFT plots are analyzed and presented. Simulations were performed using MATLAB – SIMULINK. Simulation results such as output voltage, output current and speed torque characteristics are shown. Carrier Overlapping (CO) PWM is found to execute relatively higher fundamental RMS component.

Keywords: *CO, IM, PD, PWM, THD*

1. Introduction

Multi Level Inverters have made headway in nowadays owing to their advanced advantages. It uses high voltage and current applications in recent days. The desired staircase waveform is received by separate DC voltage sources. Cascaded Multi Level Inverter is the best for compared all other kinds of multilevel inverter due to their advantages of less power circuit components, increasing output voltage level and etc. Only 10 switches and 4 DC voltage sources are utilized to develop symmetrical three phase nine-level inverter. Abdullah *et al.*, (2014) proposed an active front-end solution to balance the dc-link capacitor voltage for five-level diode-clamped inverter and the capacitor voltage balance performance by using a three-level boost converter connected with two inner capacitors and extra balanced circuits at the other two outer capacitors. Aguirre *et al.*, (2013) presented to build with selfsame modules where all inductors carry the same amount of current, simplifying the construction and operation of industrial applications with higher efficiency. Batschauer *et al.*, (2012) proposed the circuit connection which has a large portion of energy can be upgraded by the VSI (Voltage Source Inverter) by working a single multi-pulse rectifier, while the small power shares can be processed within the half-bridge modules. Cecati *et al.*, (2010) proposed the converters for photovoltaic (PV) systems usually contains two states: a dc to dc booster or stepper and a PulseWidth Modulated (PWM) inverter and these cascaded converters provide efficiency issues, interactions between its states, and problems with the Maximum Power Point Tracking (MPPT). Chaturvedi *et al.*, (2011) presented multilevel inverters which are used to come down the harmonics and there to be achieving high voltage, high-power capability with high switching due to increased device count but it can be reduced by either soft switching techniques or by modifying modulation technique employing space vector PWM techniques or sinusoidal PWM techniques. Ewanchuk *et al.*, (2011) presented a three-phase high-speed electrical machines having a low per-unit leakage

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reactance that can be reduces the voltage blocking requirement, the neutral-point-clamped (NPC) variant of the coupled inductor (CI) inverter topology (NPC-CI) is more suitable for high DC bus voltages. Hagiwara *et al.*, (2013) intended start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter based on double-star chopper cells and a square-wave method to suppress the peak circulating current. Kavousi *et al.*, (2012) intended Bee optimization method for harmonic evacuation in a CMLI and the main objective of selective harmonic elimination pulsewidth modulation strategy is evacuating lower order harmonics by clearing nonlinear equations, while the fundamental component is filled. Roshan Kumar *et al.*, (2014) presented a three-level common-mode voltage eliminated inverter with single dc supply using flying capacitor inverter and cascaded H-bridge and the three phase space vector polygon formed by this configuration and the polygon formed by the common-mode eliminated states. Wanmin Fei *et al.*, (2010) proposed a novel generalized calculation of half-cycle symmetry SHE-PWM problems for multilevel inverters and the advantages of the proposed calculation include format simplicity, flexibility in PWM waves. This three-phase nine level inverter is proposed for reduction of power electronic components and gives better THD performance.

2. MultiLevel Inverter

The proposed multi level inverter will perform better to obtain less THD and higher relative fundamental RMS and peak values. Multilevel inverter produces staircase or stepped waveform from separate DC voltage sources by synthesizing the AC sine waveform. THD decreases while number of components and voltage sources decreases. High-voltage and high-power capability applications are employed. Figure 1 show a sample proposed three phase nine level inverter using R-load.

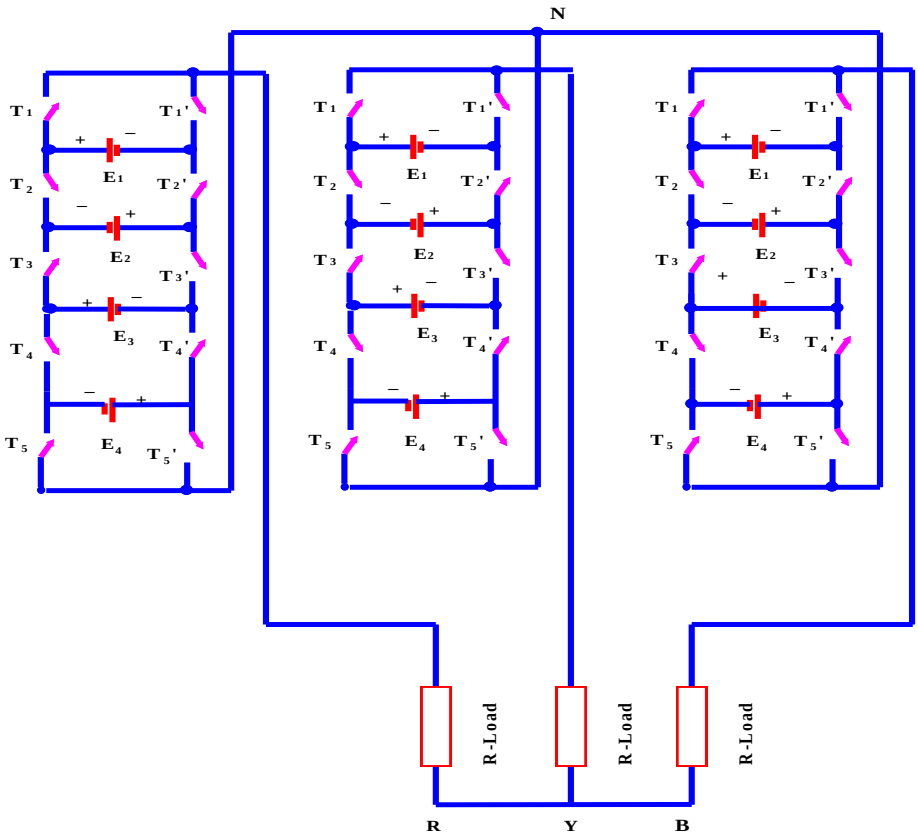

Figure 1. Proposed Three-Phase Nine Level Inverter using R-load

Operation of proposed MLI as followed: there ten power electronic switches and four DC voltage sources are used to develop nine level inverter. The stepped output voltages are like $+3V_{DC}$, $+2V_{DC}$, $+V_{DC}$, $0V_{DC}$, $-3V_{DC}$, $-2V_{DC}$ and $-V_{DC}$. The operation can be explained as: For $+4V_{DC}$ output switches T_1, T_3, T_5,T_2' and T_4' should be in ON position. For $3V_{DC}$ output switches T_1, T_3, T_2', T_4' and T_5' should be in ON position. For +2Vdc output switches T_1, T_3, T_4, T_5 and T_2' should be in ON position. For $+V_{DC}$ output switches T_1, T_2', T_3', T_4' and T_5' should be in ON position. Same as for 0Vdc output switches T_1', T_2', T_3', T_4' and T_5' should be in ON position. The negative polarity output voltages $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$ and $-V_{DC}$ are redundancy for positive polarity output voltages. MLI has applications of adjustable speed drives and renewable energy sources (solar cell, Fuel cell, wind energy and etc.).The chosen control strategy uses inverted sine carriers which are placed above zero reference. The fundamental frequency sine and trapezoidal are selected as the modulating wave. Four input dc sources with $E_1 = E_2 = E_3 = E_4 = 50$ V are used. Switches T_2, T_2', T_3 and T_3' operate at a fundamental frequency of 50 Hz while switches T_1, T_1', T_3, and T_3' operate at a frequency of 2 kHz. Thus, low-voltage-rated switches operate at high frequency and incur more switching losses, while high-voltage rated switches operate at fundamental frequency and incur more conduction losses. In this manner, the total losses among the switches get distributed. Switching losses are very directly proportional to the switching frequency.

Carrier arrangements for nine level PDPWM are shown in Figure 3 and 4 for $m_a = 0.9$.

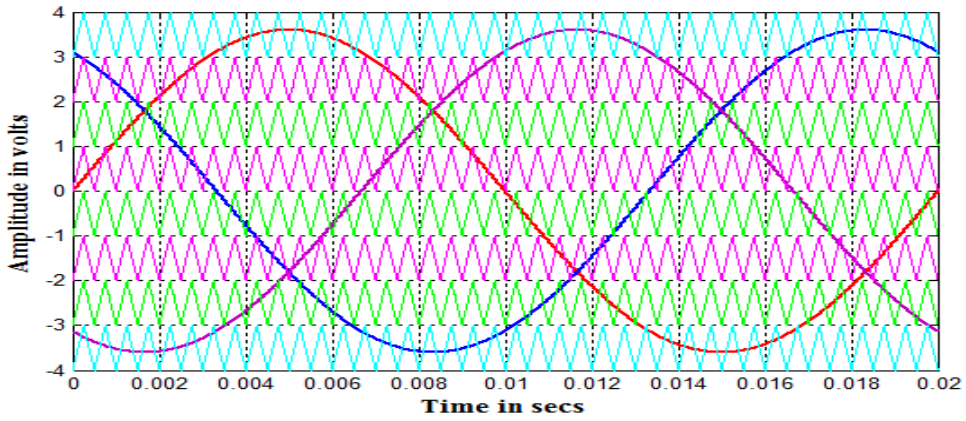

Figure 2. Carrier Arrangements for BPDPWM Strategy with sine Reference ($m_a = 0.9$, $m_f = 40$)

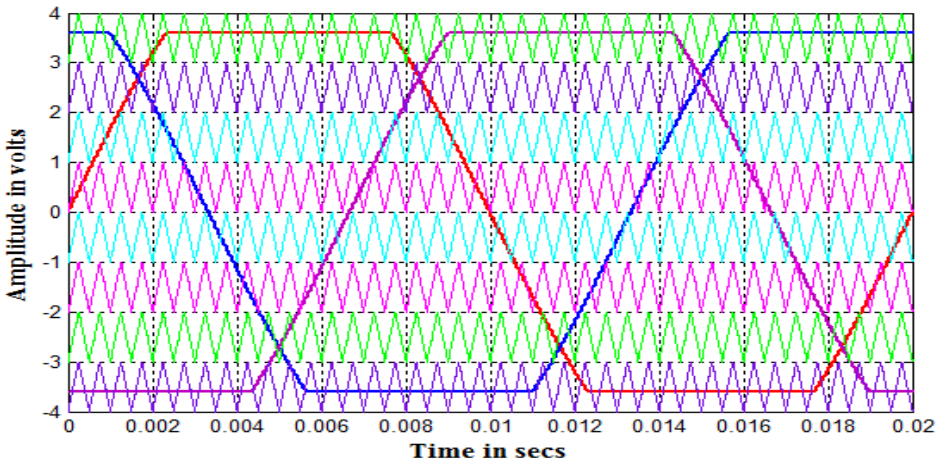

Figure 3. Carrier Arrangements for BPDPWM Strategy with 60^o Reference ($m_a = 0.9$, $m_f = 40$)

3. Simulation Results

The three-phase cascade nine-level inverter using R, RL and IM loads can be modeled in SIMULINK model by using power system block set. Switching signals for CMLI are developed using Bipolar PWM techniques but for only one sample technique BPDPWM is used for both the references. The power balancing for all among input DC sources is important so that all DC sources have equal lifetimes. Power balancing is also crucial when the DC sources are renewable sources such as PV cells or solar cells. Simulations are performed for different values of ma ranging from 0.8 – 1. The corresponding %THD values of three-phase voltage are measured for all loads using FFT block and they are shown in below figures display the V_{RMS} of fundamental and peak value of inverter output voltage for same modulation indices. Figures 4, 5 and shows the simulated nine level output (phase and line) voltages, output current, speed and torque and also corresponding FFT plots with BPDPWM strategy with sine reference but for only one sample value of ma = 0.9. Figures 4, 5, 6 and 7 shows the simulated nine level output voltage and current and also the speed, torque generated by BPDPWM strategy for both references with line and phase voltages and fundamental RMS, peak values (voltage and current) plots are shown in Figure 8-10.

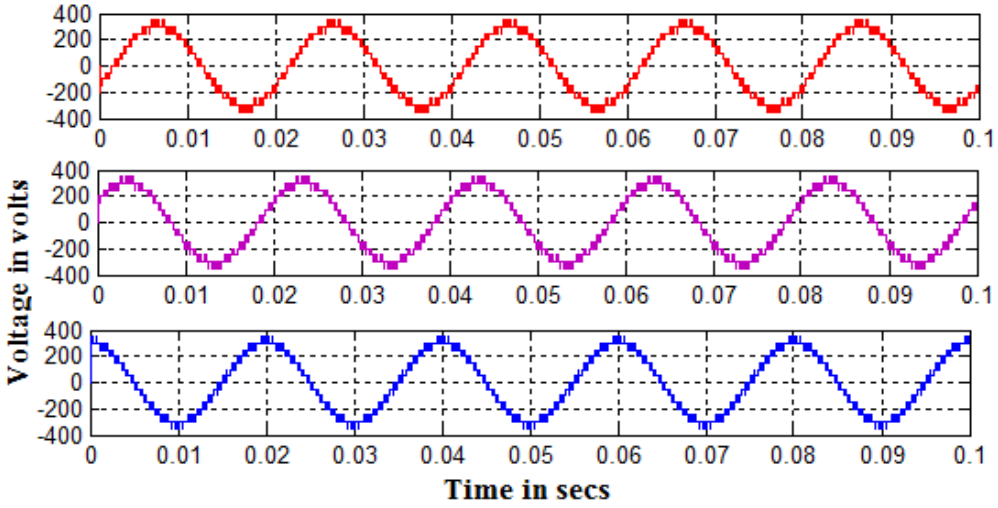

Figure 4. Output Line Voltage V_L Generated by BPDPWM Strategy for sine Reference using R-load

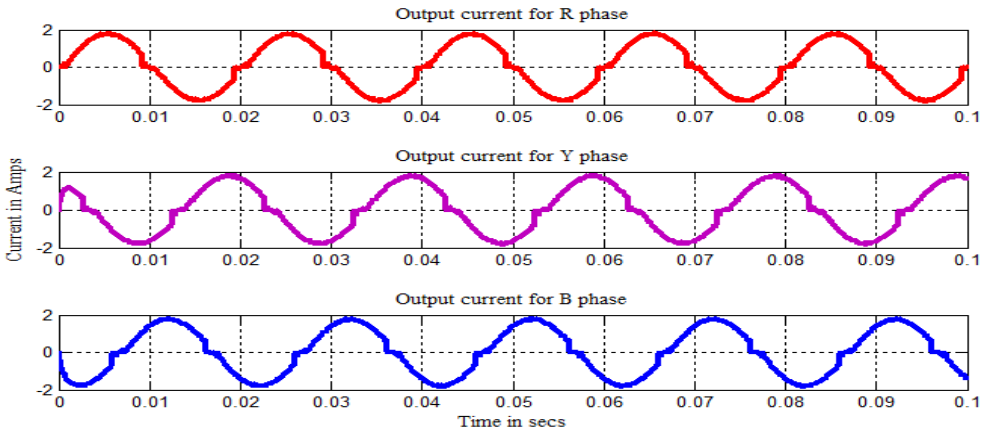

Figure 5. Output Current Generated by BPDPWM Strategy for sine Reference using RL-load

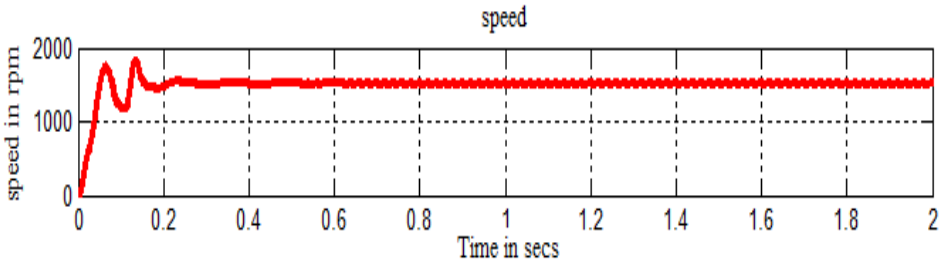

Figure 6. Speed Generated by BPDPWM Strategy for 60^0 Reference using IM Load

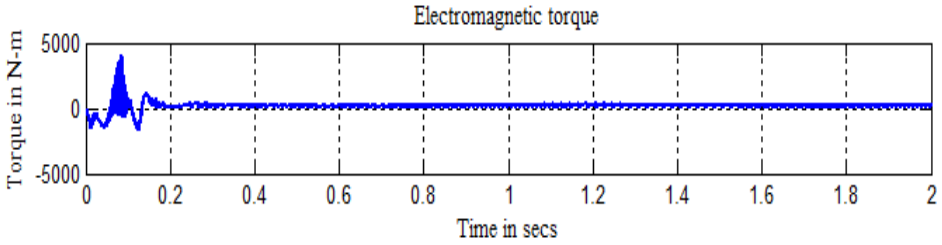

Figure 7. Torque Generated by BPDPWM Strategy for 60^0 Reference using IM Load

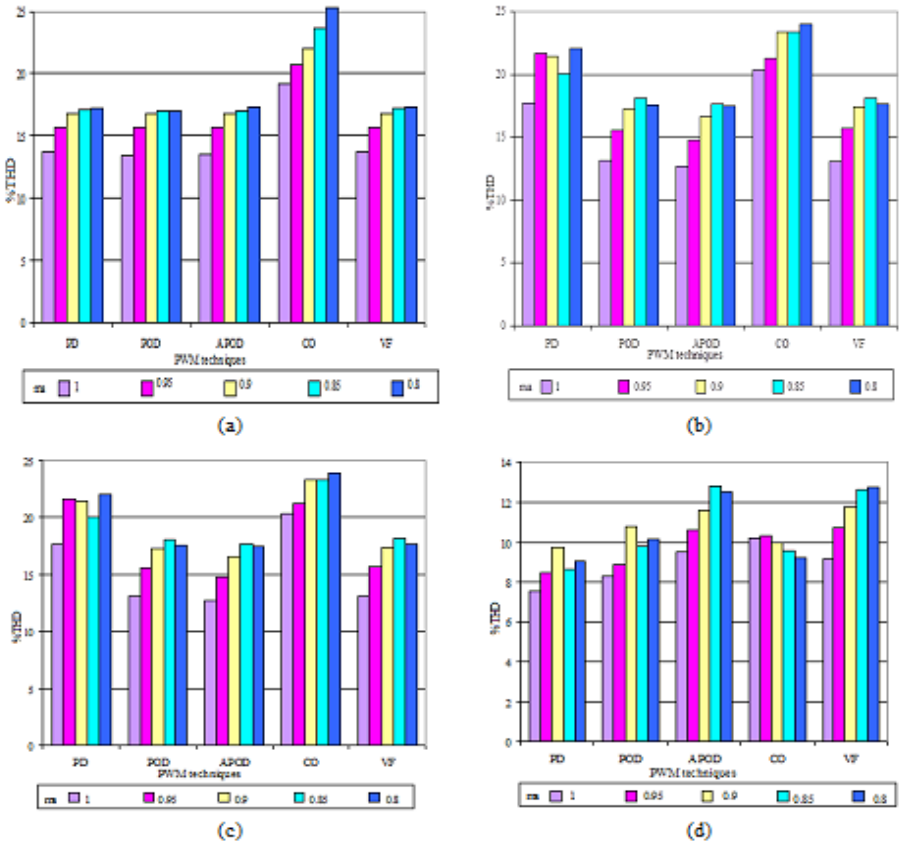

Figure 8. %THD for various Modulation Indices using R-load (a) Plot for Phase Voltage with use of Sine Reference (b) Plot for Line Voltage with Use of Sine Reference (c) Plot for Phase Voltage with Use of 60^0 Reference (d) Plot for Line Voltage with Use of 60^0 Reference

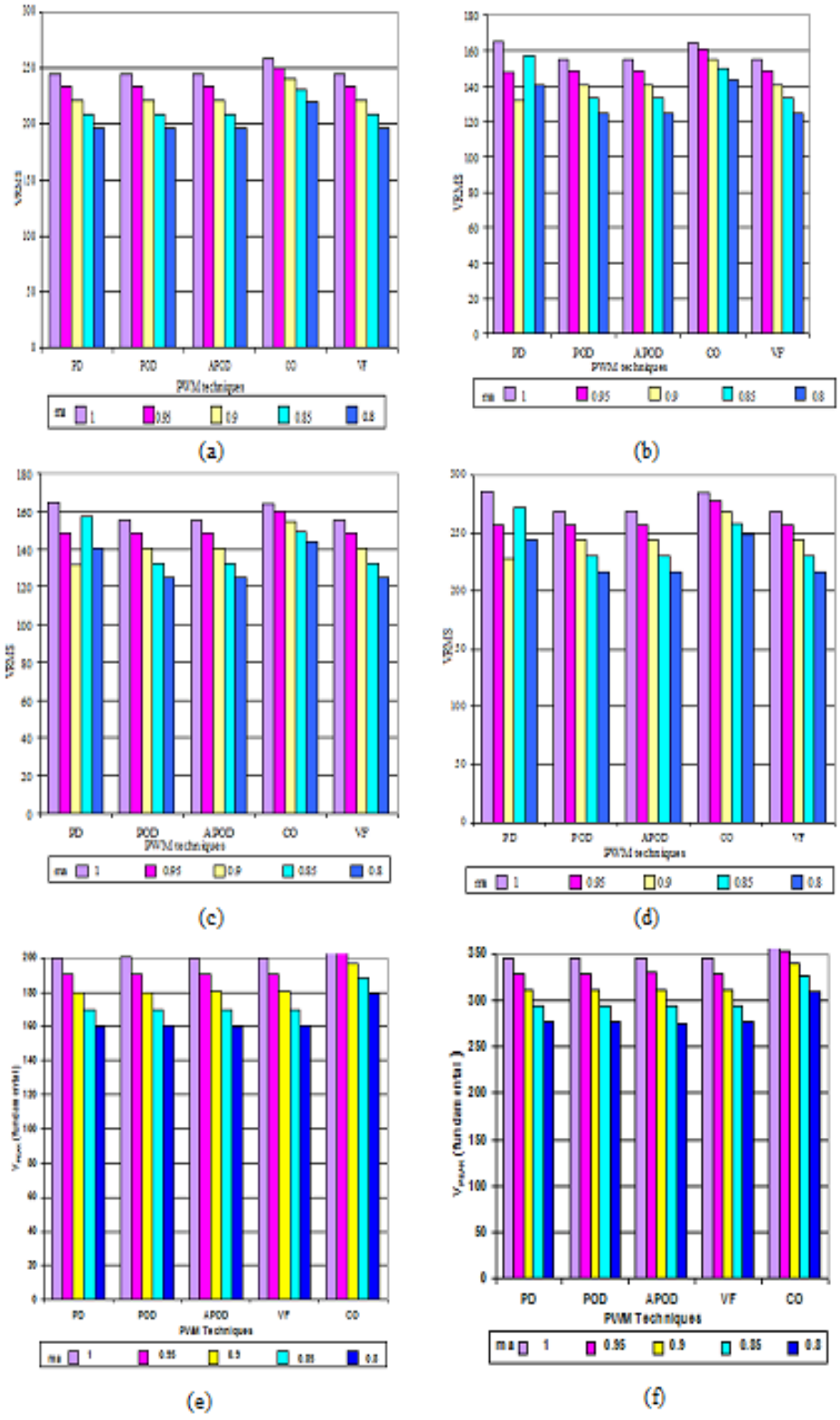

Figure 9. Showing Simulation Results for Various Modulation Indices using R-loads (a) plot for V_{RMS} (Phase Voltage) with Use of Sine Reference (b) Plot for V_{RMS} (Line Voltage) with Use of 60^0 Reference (c) Plot for V_{RMS} (Phase Voltage) with Use of Sine Reference (d) Plot for V_{RMS} (Line Voltage) with Use of 60^0 Reference (e) Plot for V_{PEAK} with Use of Sine Reference (f) Plot for V_{PEAK} with Use of 60^0 Reference

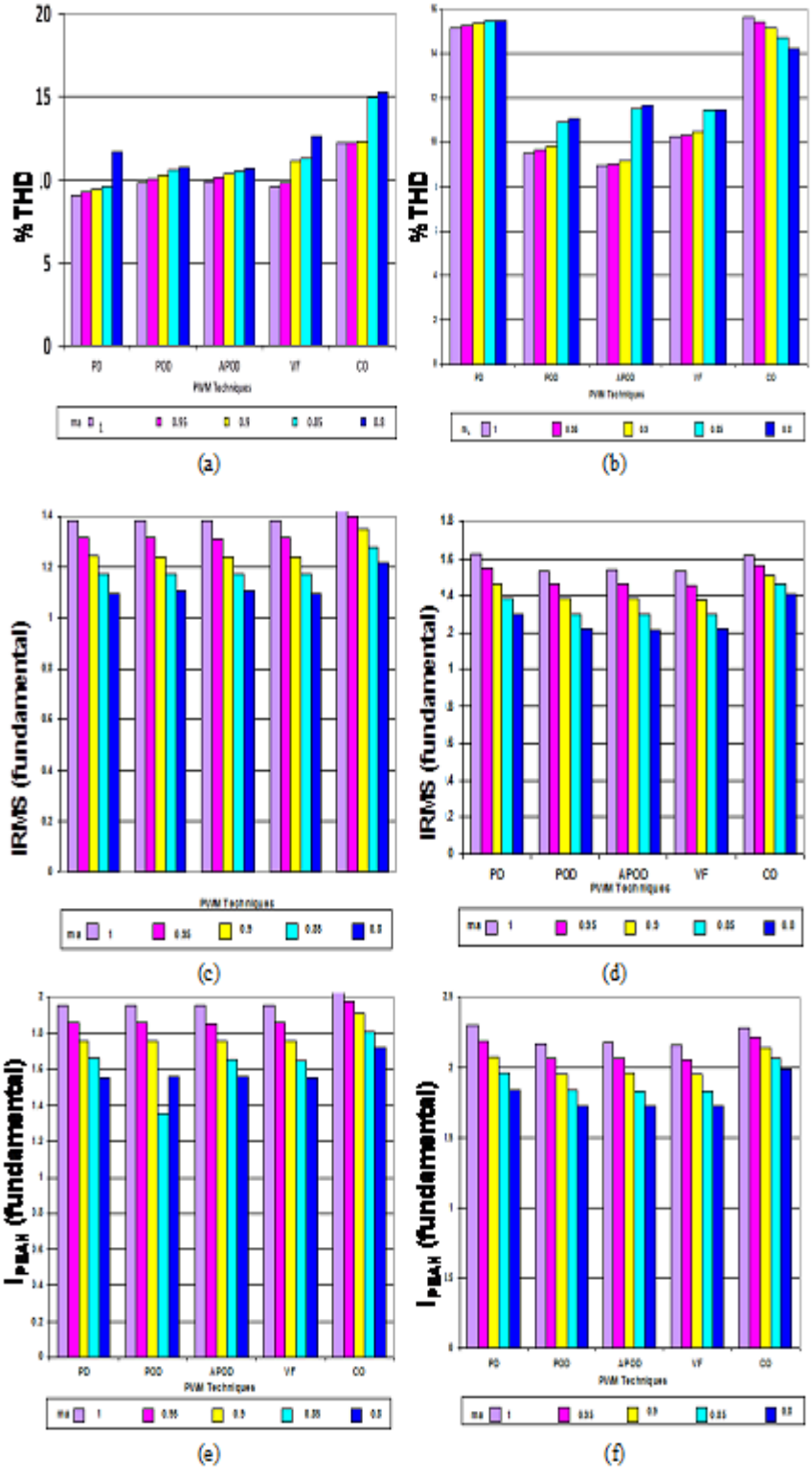

Figure 10. Showing Simulation Results for Various Modulation Indices using RL-loads (a) Plot for %THD with use of Sine Reference (b) Plot for %THD with Use of 60^0 Reference (c) Plot for I_{RMS} with Use of Sine Reference (d) Plot for I_{RMS} with Use of 60^0 Reference (e) Plot for I_{PEAK} with use of Sine Reference (f) Plot for I_{PEAK} with Use of 60^0 Reference

4. Conclusions

Comparison of THD's for all PWM techniques were showed in figures. Provides better harmonic distortion by PDPWM and APOPWM strategies and also COPWM provides fundamental higher V_{RMS}, I_{RMS}, V_{PEAK} and I_{PEAK} for R and RL loads. Rated speed N and corresponding electromagnetic torque T can be obtained by using Induction Motor as load. By comparing with conventional CMLI proposed topology contains lesser power electronic components to produce same level output.

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Authors

Dr. C.R.Balamurugan was born in 1978 in Kumbakonam. He has obtained B.E (Electrical and Electronics) and M.E (Power Electronics and Drives) degrees in 2000 and 2005 respectively from Arunai Engineering College, Tiruvannamalai and Sathyabama University, Chennai and then Ph.D in Power Electronics from Annamalai University, Chidambaram in 2015. He has been working in the teaching field for about 10 years. His areas of interest include power electronics, electrical machines and solar energy systems. He has 30 publications in international journals. His research papers 25 have been presented in various/IEEE international/national conferences. Currently, he is working as Associate Professor in the Department of EEE, Arunai Engineering College, Tiruvannamalai. He is a life member of Indian Society for Technical Education. Contact number-+91-9894522351. E-mail:crbalain2010@gmail.com.

Dr. S.P.Natarajan was born in 1955 in Chidambaram. He has obtained B.E (Electrical and Electronics) and M.E (Power Systems) degrees in 1978 and 1984 respectively from Annamalai University securing distinction and then Ph.D in Power Electronics from Anna University, Chennai in 2003. He is currently Professor and Head of Instrumentation Engineering Department at Annamalai University where he has put in 31 years of service. He produced eight Ph.Ds and presently guiding eight Ph.D Scholars and so far guided eighty M.E students. His research papers 66 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 20 publications in national journals and 43 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of permanent magnet brushless DC motor, embedded control for multilevel inverters and matrix converters etc. He is a life member of Instrument Society of India and Indian Society for Technical Education. Contact number- +91-9443185211. Email: spn_annamalai @rediffmail. com.

Dr. R.Bensraj was born in 1973 in Marthandam. He has obtained B.E (Electrical and Electronics), M.E (Power Systems) and Ph.d (Multilevel Inverter) degrees from Annamalai University, Chidambaram. He has been working in the teaching field for about 13 years. His areas of interest include power electronics, electrical machines and solar energy systems. He has 32 publications in international journals. His research papers 10 have been presented in various/IEEE international/national conferences. Currently, he is working as Associate Professor in the Department of EEE, Annamalai University, Chidambaram. He is a life member of Indian Society for Technical Education. Contact number- +91-9443929992. E-mail:bensraj_au@rediffmail.com.

Dr. B.Shanthi was born in 1970 in Chidambaram. She has obtained B.E (Electronics and Instrumentation) and M.Tech (Instrument Technology) from Annamalai University and Indian Institute of Science, Bangalore in 1991 and 1998 respectively. She obtained her Ph.D in Power Electronics from Annamalai University in 2009.She is presently a Professor in Central Instrumentation Service Laboratory of Annamalai University where she has put in a total service of 22 years since 1992.Her research papers (30) have been presented in various / IEEE international /national conferences. She has 3 publications in national journal and 35 in international journals. Her areas of interest are: modeling, simulation and intelligent control for inverters. Contact number- +91-9443185211. Email: shancisl@ gmail. com.