

A Novel Optimal 2-D Layout for Cache Memory at 45nm CMOS Technology

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Abstract

This paper presents a novel optimal 2-D layout using PN and PNN pattern during placement, we utilize the device merging, abutment and alignment technique to enhance the wire-length and area-efficiency. A placement objective is formulated balancing the symmetry for routing and the area efficiency. To the best of my knowledge, this is the first piece of work that can handle PN and PNN pattern for placement and using device merging, abutment and alignment technique simultaneously. Two cell (MTIP3&IP3) are used to demonstrate the effectiveness of approach. Moreover, the proposed method generates more area-efficient transistor placements than the conventional method. In experiment we applied PN and PNN pattern for placement of devices with the device merging and abutment technique to attain the results for MTIP3 and IP3 cell 6.5025umsq and 3.114umsq respectively. Result shows that the area of IP3 cell is improved by 50%.

Keywords: Abutment, Custom Design, Device Merging, Placement Technique Layout, Multi-Row Placement

1. Introduction

According to Moore's law as number of transistor increases frequently in every eighteen months. This shows that power dissipation would be a big challenge. From the past years of VLSI design, engineers are developing a number of techniques for automated design target and this automated techniques reduces the product time and increasing the robustness of the final product.

In traditional VLSI circuit design, in routing the wire moves only in horizontal and vertical direction but now a days new Steiner tree problem has introduced for tremendous study. According to these method interest in circuit designing increased, as routing of wire moves in three or four orientation. Several automatic techniques had been proposed for placement and routing, so that a great issue of design violation from layout resolved. Layout creation with 100% DRC clean has been an important topic of research for VLSI Design. Along with DRC, LVS also have an important role in IC fabrication.

A placement with shorter wire length achieved by a good placement techniques, here we are discussing number of techniques which we can used for getting an optimized wire-length, and has a higher probability that its congested region are relatively minimized. Methodology used for specifying the layout of each individual transistor, designing and the complete interconnection between is known as full custom design methodology. The performance of the chip, and the area minimization can be achieved by full custom methodology.

The rest of the paper is organized as follows. In Section 2 previous work about the placement techniques in layout. Section 3 having problem formulation. In Section 4, the method for area minimization. Experimental results will be addressed in Section 5. Finally, some conclusions and future-scope are presented in Section 6.

2. Review of Related Work

Here [2], Chidchanok Lursinsap presented folding model technique for combining a pull-up transistor with other transistors of a term then place the term so that the number of columns assigned to terms is minimal. In this work two models are: Model A- normal PLA and Model B-PLA with folding model and pull up transistor. Model A gives an acceptable result when the number of terms is lower and only two-level Boolean functions are implemented. Model B is practical, more efficient and multi-level Boolean functions. So can say that model B is more efficient than model A.

[3], Shigetoshi Nakatake has given diffusion sharing and well island generation approach for regularity-oriented analog placement. He achieved wire length shorten by 27 %, better area & computation time with well island generation. Chip area save by 8 % and wire length reduce by 29 % using given approach. Future scope is to cope with further amore practical design rules & constraints in analog layout.

In [4], Center based corner block list (c-cbl) has given by Qiang Ma, which is a natural extension of corner block list (cbl) to represent a common centroid placement of a set of device pair to maintain the performance and stability of a circuit and it is desirable to restrict all the devices of a common centroid group to form a cluster in the final placement, without interleaving with other blocks not in the same group. Experimental results show that given approach is fast and have high scalability and handle effectively, and placements satisfying the constraints can be generated efficiently with an average dead space of 8.29%.

[5] Michael Eick presented a novel symmetry computation method, introducing the structural signal flow graph to generate hierarchical placement rules, which are essential for a successful analog placement. Experimental results showed this approach generates more placement rules and can lead to better circuit performance and parametric yield according to post-layout simulation with the state-of-the-art placement tool.

3. Description of the Problem

The objective of the problem is placement of the devices using multi-row and after placement apply diffusion sharing, matching, symmetry and device merging, technique for area minimization. The first phase is the analog placement considering the device merging, matching and symmetry techniques in single row. The placement priority is set according to area requirement.

In second phase, we place the devices in multi-row considering again the device merging, matching and symmetry technique. To maintain the symmetry and the accuracy in a device routing should be done in a proper manner.

4. The Approach

In this paper, we will present a transistor placement that can handle both device merging and the symmetry technique to a practical way to generate a standard cell. Our circuit includes unequal number of P and N transistors. Placement of transistors are done according to the way we are getting minimum area, so the devices we are placed in different pattern i. PN and NP ii. PNP and NPN iii. PNP and NPNP and many more. After placement to make every transistor accessible, different techniques are used so that we get easy routing

4.1 Placement Techniques

4.1.1. Device Merging

Device merging [1] is also known as geometry sharing techniques because group will share their geometries to reduce area and wire length. In this technique the group will

merge either horizontal or vertical and merge dynamically either merge all in one group or merge in 2 different group.

Since PMOS and NMOS cannot be merge directly so there will be no device merging between PMOS and NMOS transistor. Therefore the technique is used but only in NMOS and PMOS separately. Figure 4.1 shows an example of how device merging works

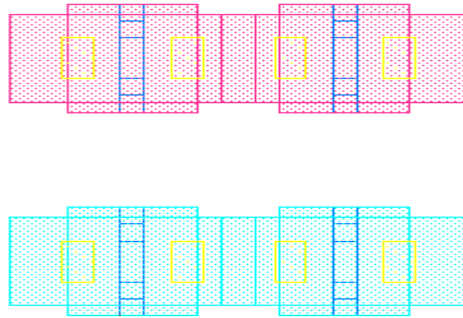


Figure 4.1. Device Merging in PMOS and NMOS

4.1.2 Abutment

In this technique two MOS transistors are abutted and have shared their diffusion region. Abutment can be done in two ways horizontally and vertically, when blocks are required to abut horizontally block1 on the left and block2 is on the right side, and if blocks abut vertically block 1 on top and block2 on bottom. Abutment only possible in same MOS transistors.

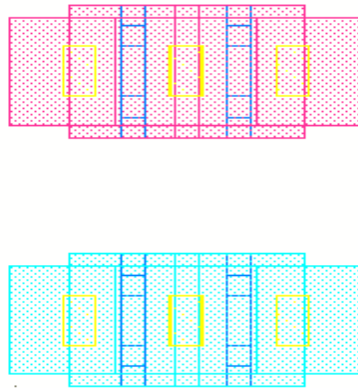


Figure 4.2. Abutment Technique

4.1.3 Alignment

In this technique MOS transistors are aligned so that the route length reduces, alignment can be done in two ways horizontally and vertically.

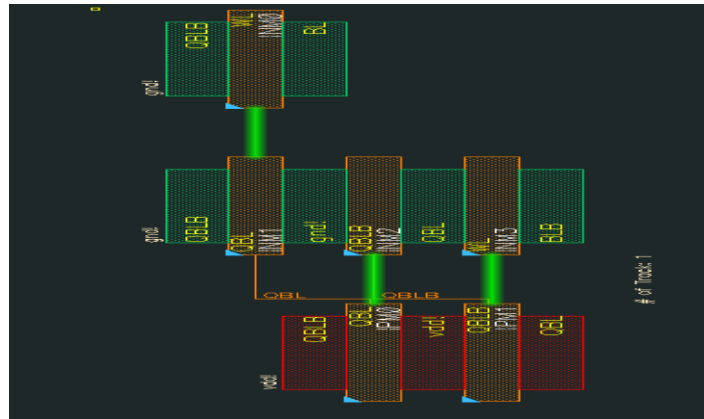


Figure 4.3. Alignment Technique

5 Experimental Results

In order to confirm effectiveness of the method, we implement techniques on IP3 cell and MTIP3 cell and carried out experiment on cadence virtuoso layout.

Table 1 shows the experimental results of IP3 and MTIP3 using two row and multi-row placement

Table 5.1. Area Results

CIRCUIT	NO OF TRANSISTORS	PLACEMENT	PATTERN	AREA
MTIP3 CELL	9	2-row	PN	7.0785umsq
MTIP3 CELL	9	Multi-row	NPN	6.5025umsq
IP3 CELL	9	2-row	NP	3.4225umsq
IP3 CELL	9	Multi-row	PNN	3.114umsq

The area of placement obtained by the proposed method is less than the automatic layout system in this experiment, all DRC violations can be legalized at cadence virtuoso layout workstation. Part of the resulting layout are presented in figures.

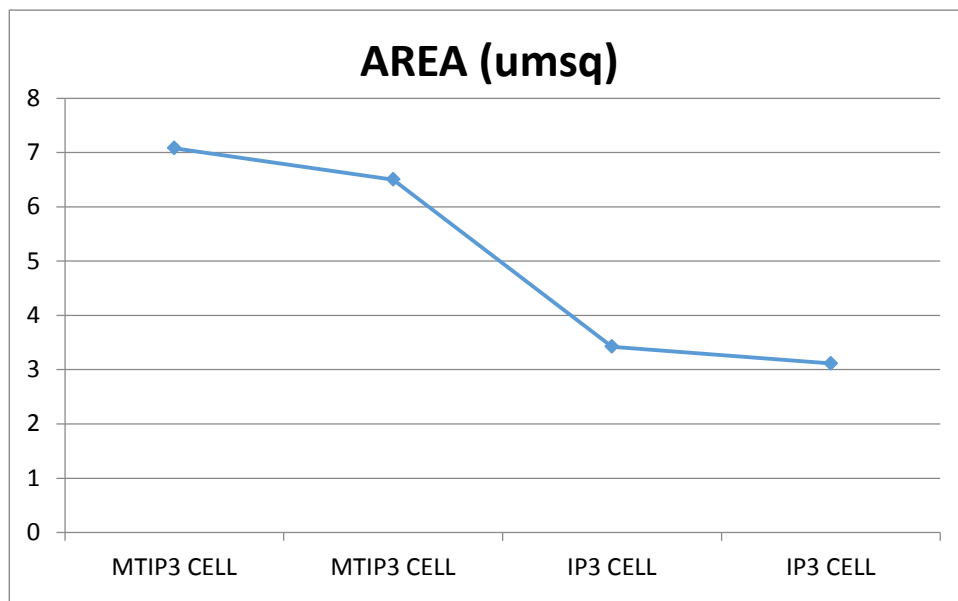


Figure 5.1. Comparison between MTIP3 and IP3

5.1.1 Schematic of MTIP3 Cell

MTCMOS [6] provides circuit designers with more opportunities to optimize circuits in performance, power and energy. In general, higher v_{th} -devices are employed in non-critical paths for reducing power while lower- v_{th} devices are adopted in critical paths for achieving higher performance. Schematic of MTIP3 cell shown in Figure 5.1

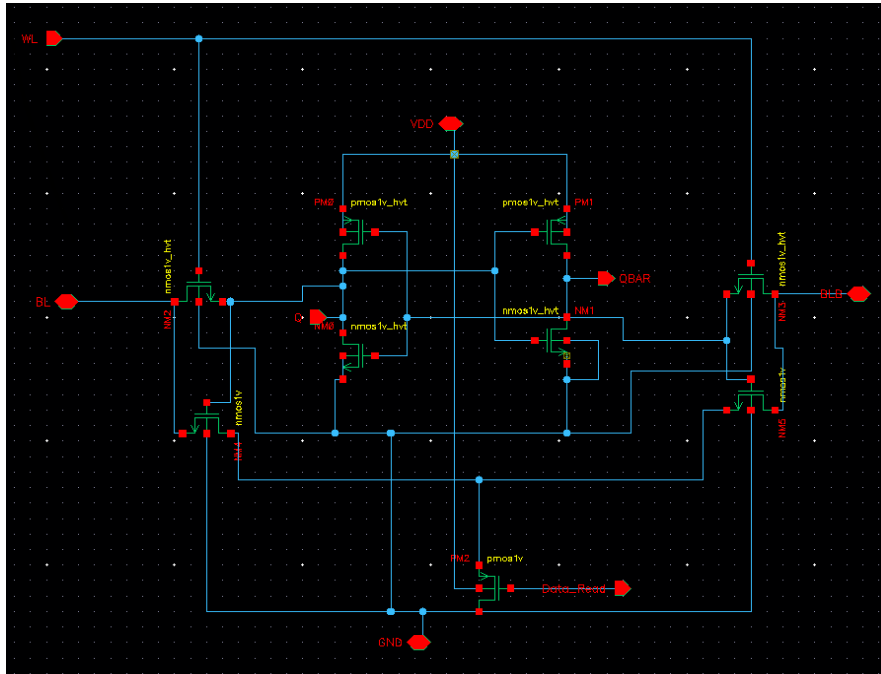


Figure 5.1. Schemataic of MTIP3 CELL

i. Layout of MTIP3 CELL

Figure shows the layout of MTIP3 using two row and having PN pattern

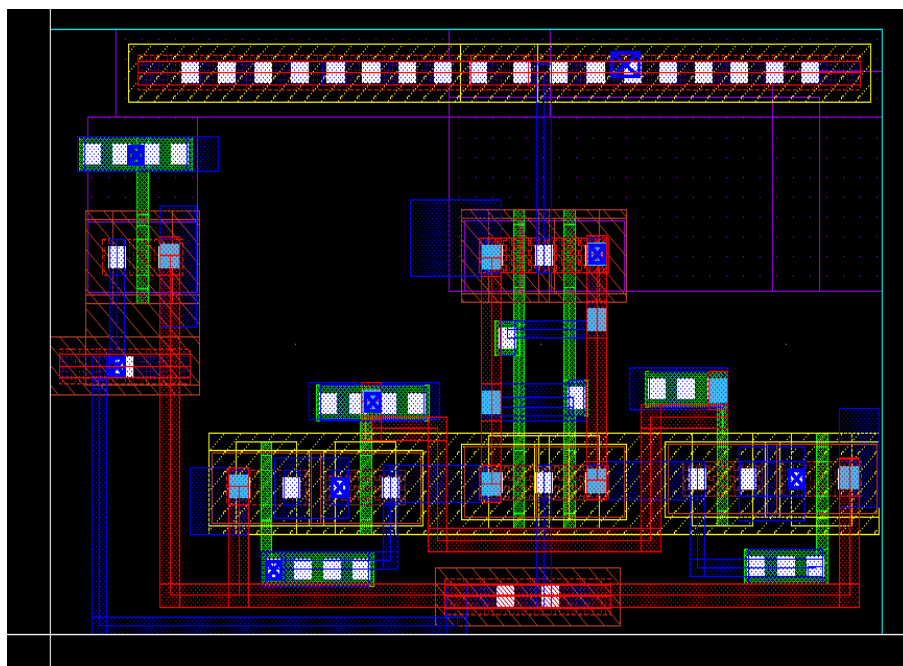


Figure 5.2. MTIP3 Layout using PN Pattern

ii. Area Report of MTIP3 using PN Pattern

```
\i ;;;;;;;;;;;;;;;;;;AREA REPORT;;;;;;;;;;;;;;;;;;;;;;;;
\a mouseSingleSelectPt()
\i 0.1:2.1
\r nil
\a mouseSingleSelectPt()
\i 0.1:2
\r t
\i css()~>??
\t (db:0x1b01cc92 cellView db:0x1b01d012 objType "PRBoundary"
\t   prop nil bBox
\t   ((0.0 0.0)
\t   (3.395 2.085)
\t   ) children
\t   nil groupMembers nil parent nil
\t   textDisplays nil assocTextDisplays nil figGroup
\t   nil markers nil numEdges 4
\t   points
\t   ((0.0 0.0)
\t   (0.0 2.085)
\t   (3.395 2.085)
\t   (3.395 0.0)
\t   ) edgeNames
\t   ("EDGE_1" "EDGE_2" "EDGE_3" "EDGE_4") area
\t   7.078575 isOrthogonal t isRectangle t
\t   blockages nil coreBoxSpec nil IOBox
\t   nil
\t )
\p >
\a hiResizeWindow(window(1) list(-4:43 1270:937))
\r t
█
\i css()~>area
\t 7.078575
\p >
\a hiQuit()
\p >
\a hiDBoxOK(hiQuitDBox)
\r t
\o
\# Memory report: on exit          162 MB, process size 541 MB at UTC 2015.04.30 09:33:46.272
\# Memory report: peak usage      162 MB, process size 541 MB
~
```

Figure 5.3. Area Report of MTIP3 using PN Pattern

iii. The layout of MTIP3 using multi-row and having NPN Pattern

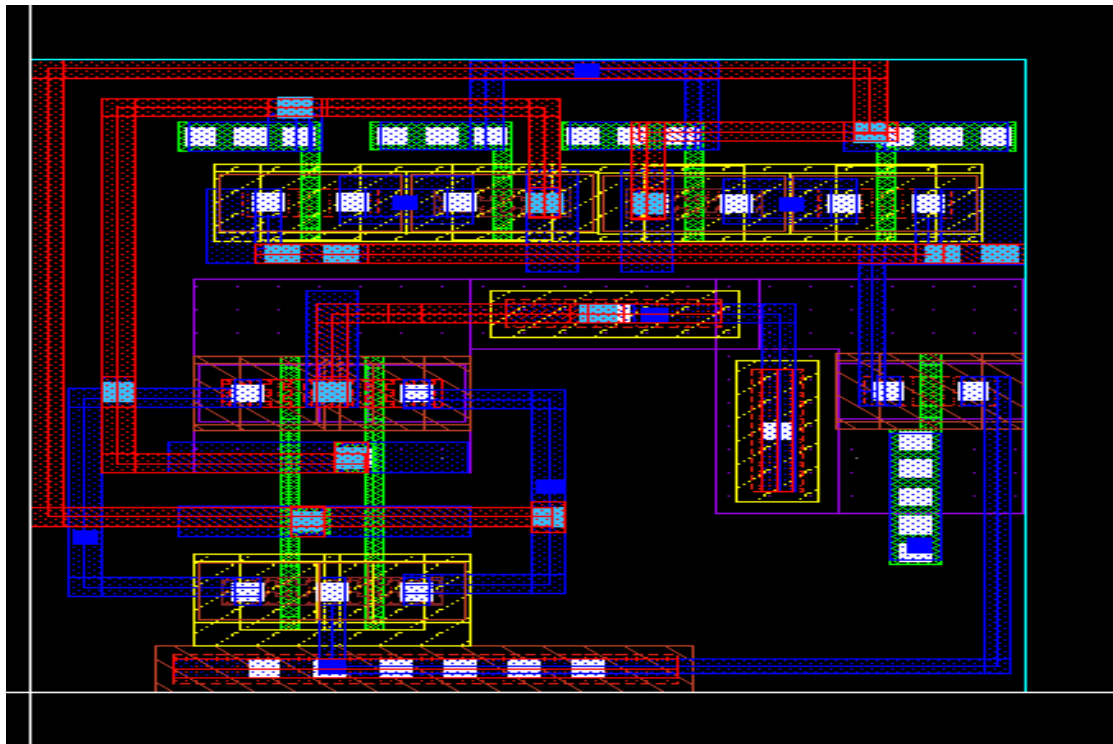


Figure 5.4. MTIP3 Layout using NPN Pattern

iv. Area Report of MTIP3 Using NPN Pattern

```
css()~>??  
(db:0x1a1cca92 cellView db:0x1a1cce12 objType "PRBoundary"  
 prop nil bbox  
  ((0.0 0.0)  
  (2.415 2.7)  
 ) children  
 nil groupMembers nil parent nil  
 textDisplays nil assocTextDisplays nil figGroup  
 nil markers nil numEdges 4  
 points  
  ((0.0 0.0)  
  (0.0 2.7)  
  (2.415 2.7)  
  (2.415 0.0)  
 ) edgeNames  
  ("EDGE_1" "EDGE_2" "EDGE_3" "EDGE_4") area  
  6.5205 isOrthogonal t isRectangle t  
  blockages nil coreBoxSpec nil IOBox  
  nil  
 )  
css()~>area  
6.5205
```

Figure 5.5. Area Report using NPN Pattern

5.1.2 IP3 Cell

IP3 [7] SRAM bit-cell is also known as low stress SRAM cell. It has 2 separate sub-cell for write and read, where write sub cell has dual role of data write and data hold. IP3 SRAM bit cell structure presented using drowsy scheme and pmos stacking with ground. This cell reduces the power consumption with the small area penalty. The stack transistor is used one per row in the memory array so that area penalty of this transistor can be reduced. Figure shows the schematic of IP3 Cell.

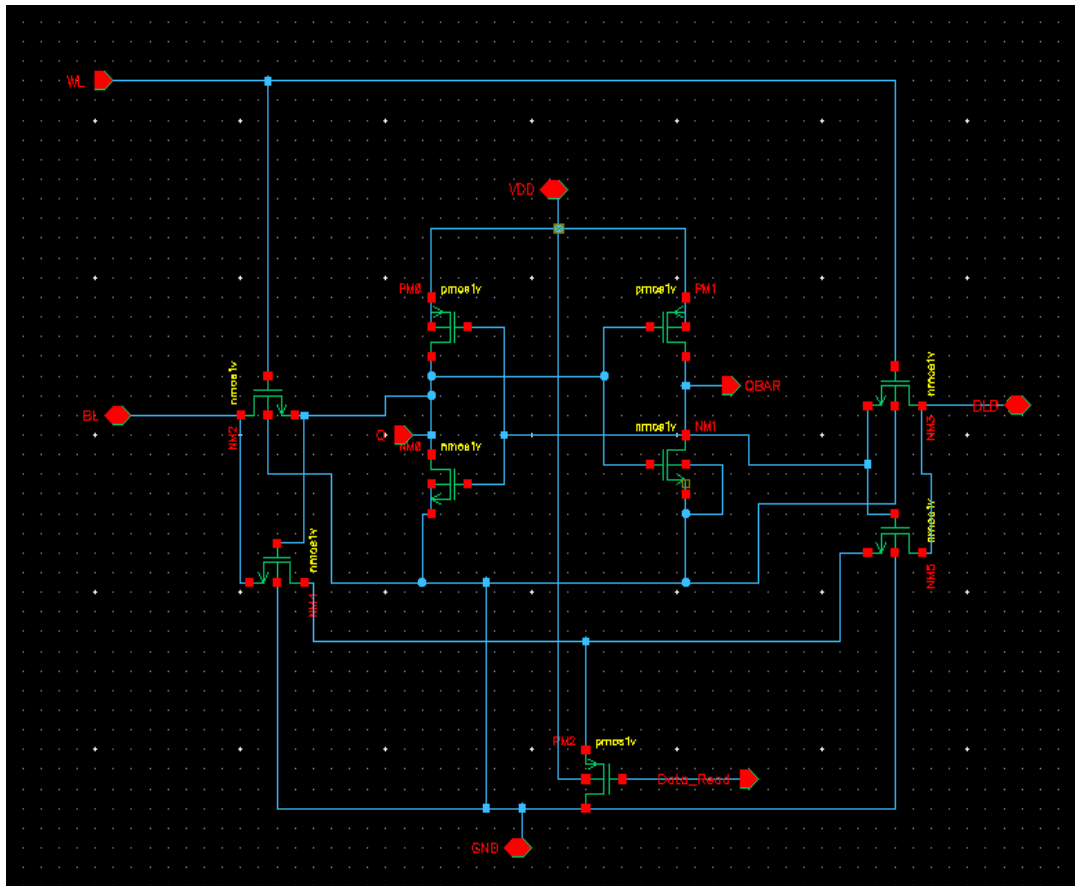


Figure 5.6. Schemtaic of IP3 Cell

i. Layout of IP3 CELL

Figure shows the layout of IP3 using two row and having NP pattern

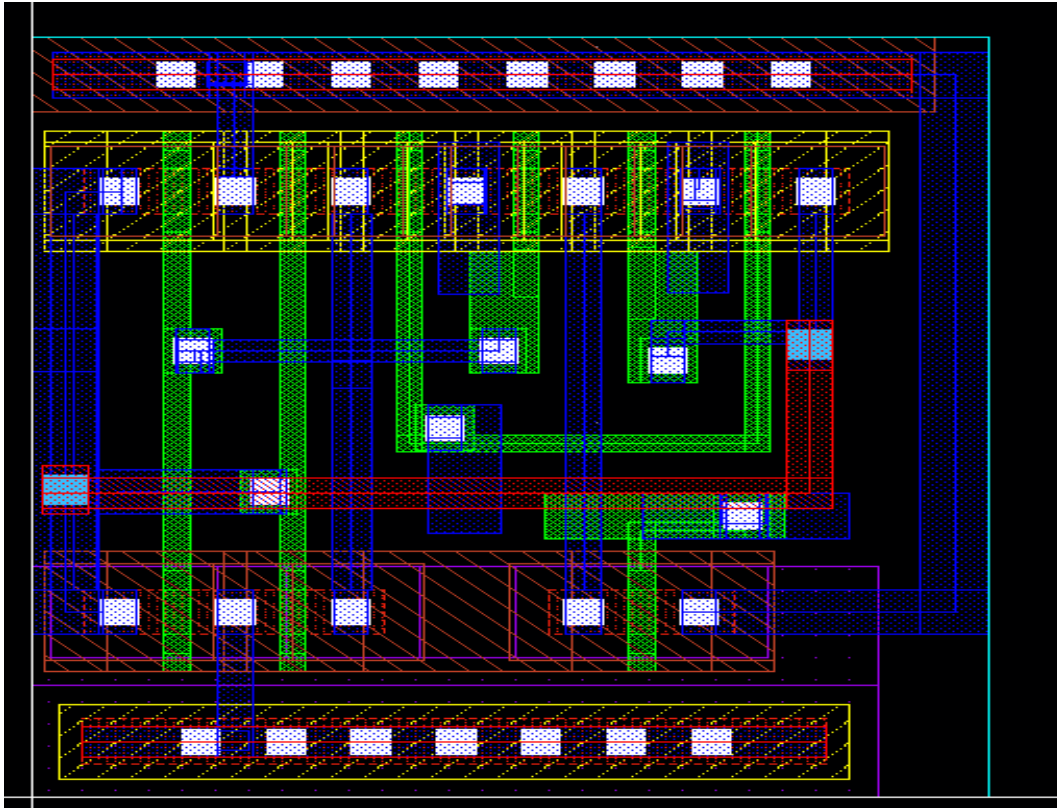


Figure 5.7. IP3 Layout using NP Pattern

ii. Area report of IP3 using NP Pattern

```
css()~>??  
(db:0x1a1cd612 cellView db:0x1a1cce12 objType "PRBoundary"  
  prop nil bBox  
    ((0.0 0.0)  
     (1.69 2.025)  
  ) children  
  nil groupMembers nil parent nil  
  textDisplays nil assocTextDisplays nil figGroup  
  nil markers nil numEdges 4  
  points  
    ((0.0 0.0)  
     (0.0 2.025)  
     (1.69 2.025)  
     (1.69 0.0)  
  ) edgeNames  
    ("EDGE_1" "EDGE_2" "EDGE_3" "EDGE_4") area  
    3.42225 isOrthogonal t isRectangle t  
    blockages nil coreBoxSpec nil IOBox  
    nil  
)  
css()~>area  
3.42225
```

Figure 5.8. Area Report of IP3 Cell using NP Pattern

iii. The layout of IP3 using multi-row and having PNN Pattern

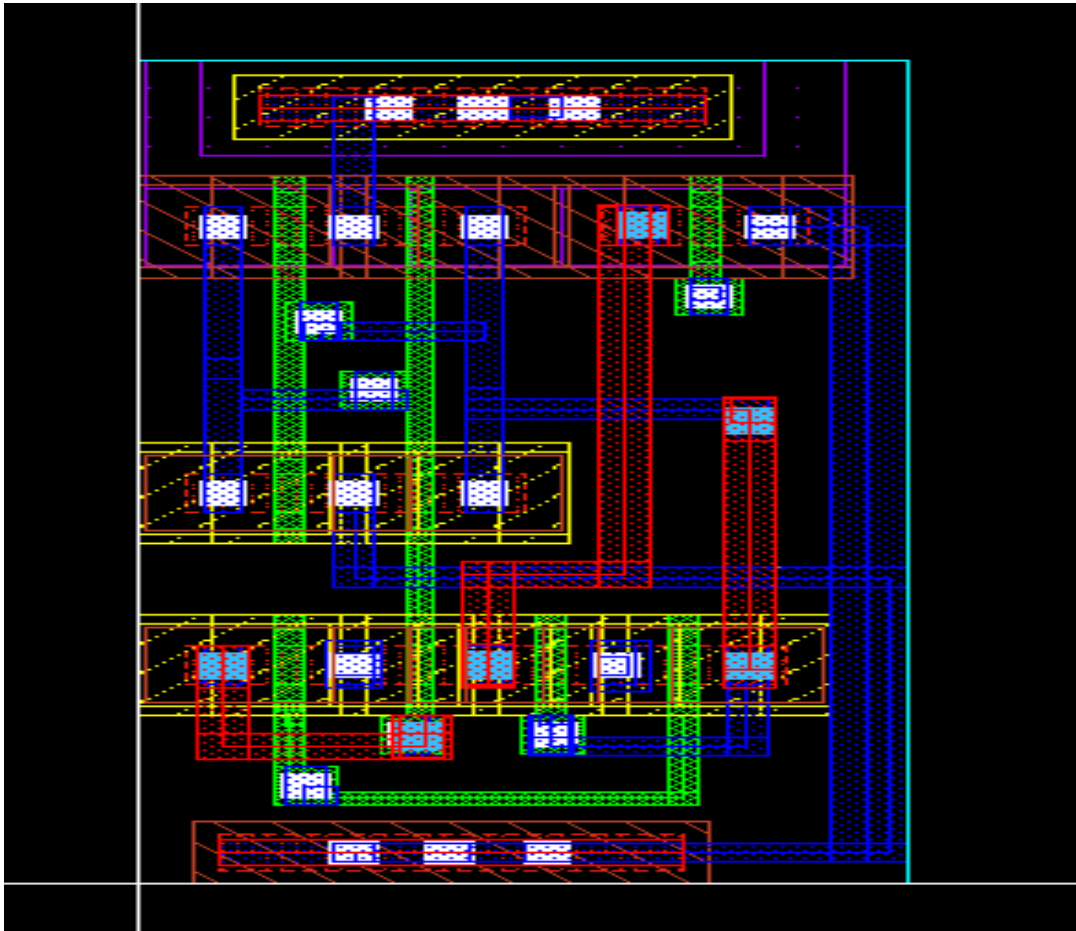


Figure 5.9. IP3 Layout using PNN Pattern

iv. Area report of IP3 using PNN Pattern

```
css()~>??  
(db:0x1a1cd12 cellView db:0x1a1cce12 objType "PRBoundary"  
 prop nil bbox  
  ((0.0 0.0)  
   (1.2 2.595)  
  ) children  
 nil groupMembers nil parent nil  
 textDisplays nil assocTextDisplays nil figGroup  
 nil markers nil numEdges 4  
 points  
  ((0.0 0.0)  
   (0.0 2.595)  
   (1.2 2.595)  
   (1.2 0.0)  
  ) edgeNames  
 ("EDGE_1" "EDGE_2" "EDGE_3" "EDGE_4") area  
 3.114 isOrthogonal t isRectangle t  
 blockages nil coreBoxSpec nil IOBox  
 nil  
)  
css()~>area  
3.114
```

Figure 5.10. Area Report of IP3 using PNN Pattern

6. Conclusion and Future Scope

In this, some recent topological approaches to placement techniques have been surveyed, and we have analyzed both layouts to find their area when implementing different techniques multi row pattern layout gives an acceptable result. Extensive experimental results demonstrated the effectiveness of approach. This placement of devices and the corresponding layout using different techniques have been implemented on Cadence Virtuoso Layout. The results showed that considering different techniques together outperformed the amount of area by 50% on average.

MTIP3 cell having low power utilization as compare to IP3 cell, in MTIP3 the multi vth devices are used where as in IP3 same vth devices are used. While minimizing an area we conclude that the IP3 cell having less area utilization as compare to MTIP3 due to multi vth device in MTIP3 the area of chip increases.

Our future work will focus on minimizing power during layout. Further techniques can be used to minimize power during layout.

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