

A 43 μ watt 3-bit Flash ADC designed with TMCC and Bit Referenced Encoder in 180 nm CMOS Technology

Aditi Kar¹ and Alak Majumder²

¹Department of ETCE, Tripura Institute of Technology Agartala -791112

²Department of ECE, National Institute of Technology, Arunachal Pradesh,
Yupia – 799009, India

akar0412@gmail.com, majumder.alak@gmail.com

Abstract

The analog-to-digital converter (ADC) is an essential part of system-on-chip (SoC) products because it bridges the gap between the analog physical world and the digital logical world. In the digital domain, low power and low voltage requirements are becoming more important issues as the channel length of MOSFET shrinks below 0.25 sub-micron values. Moreover, SoC trends force ADCs to be integrated on the chip with other digital circuits. These trends present new challenges in ADC circuit design. Thus, this thesis is to investigate high speed, low power, and low voltage CMOS flash ADCs for SoC applications. In this paper an area efficient low power high Speed 3-bit Flash Type ADC using bit referenced encoder is proposed in 180 nm CMOS technology. The concept of Threshold Modified Comparator Circuit (TMCC) is also introduced as a modification of the conventional comparator. The proposed design of the ADC occupies an active area of 0.0036 mm² and consumes 43.146 μ W of Average Power while operating with an input frequency (f_{in}) of 10 MHz and a supply voltage of 1.8 Volt.

Keywords: Flash Type ADC, Comparator, TMCC, Threshold voltage, Multiplexer, Bit referenced encoder

1. Introduction

Analog to digital converters are used to convert real world analog signals into digital representations of those signals. Digital signal processing can then efficiently extract information from the signals. ADCs find use in communication, video, audio, sensors and many other applications. High speed (Multi-GHz sampling rate), low resolution ADCs are used in high speed wire line and wireless communications, digital oscilloscopes and radar. Flash architecture is typically used for high speed ADC [1]. ADCs span a large range of speeds and resolutions, from low speed, high resolution ADCs to high speed low resolution ADCs. Different ADC architectures lend themselves to different application spaces.

The Figure 1 depicts sampling rate v/s resolution space occupied by common ADC architectures.

Analog circuits are often used in more power constrained situations. Microprocessor and SoC designs may encounter thermal limits of power dissipation or have low power targets for use in 'Green' products. The power consumption of digital CMOS logic is proportional to the square inverse of scaling factor (k) [2].

$$\text{Digital Power} \propto k^{-2} \quad (1)$$

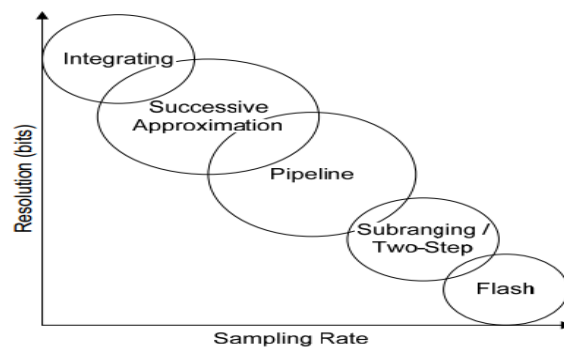


Figure 1. Conceptual view of Sampling Rate v/s Resolution Space

However, analog power of CMOS flash ADC scales with the inverse of scaling factor when bandwidth is held constant [3].

$$\text{Analog Power} \propto k^{-1} \quad (2)$$

The digital power scales faster than the analog power as the CMOS technology advances, making the use of digital logic to reduce analog complexity increasingly attractive. This has led to a great deal of research on digital techniques to improve the performance of simple, low resolution analog circuits in ADCs, resulting in ‘Mostly Digital’ analog circuits [4].

As the comparators used in architecture are in parallel, the flash architecture is a better option for high speed ADCs, but in terms of power consumption issues it is not that much of efficient. If we talk about latency, flash type ADC is the most appropriate candidate. Flash ADCs in particular suffer significantly from random mismatch. Each of the comparators operating in parallel has its own random offset resulting from random mismatches between comparators. The random offsets create non-linearity in the ADC transfer function, thereby distorting the output. Control of comparator random offset is essential to create accurate flash ADCs. A conventional flash type ADC is shown in Figure 2. The series connected resistors are working as voltage divider network thereby consuming a huge amount of static power. Also the no. of used components of a Flash Type ADC increases as resolution increases [5]. The conventional Flash ADC uses comparator composed of uncompensated operational amplifier having large number of transistors leading to large area and large power dissipation.

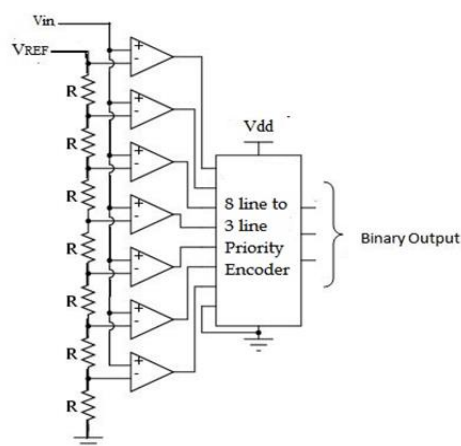


Figure 2. Architecture of the Conventional Flash Type ADC

2. Related Work

In last 2 decades, so many works has been done on low power ADC so as to digitize the real analog world signals. Every year higher and higher sampling rate as well as lower and lower power dissipations are reported in the literature. High speed, low power, lower chip area, low aperture jitter etc. are the important parameters by means of which performance of an ADC is analysed. Among these, low power dissipation is one of the main threats for the researchers. Power dissipation occurs mainly because Transistor Matching, Device Parasitic and Calibration of Designed ADC.

The TIQ technique has been used thereby replacing resistor bank of conventional method to design a flash ADC [6]. A capacitive interpolation technique has been used to have a low power design [7]. Use of digital techniques instead of analog techniques was employed to overcome comparator offset [8]. In 2002 an average termination circuit is proposed to reduce the number of over-range amplifiers thereby reducing the power consumption [9]. An ADC is designed for disk-drive read channel applications [10]. A new technique named current interpolating technique is implemented to design an ADC operating at 1V power supply [11]. In another edition the authors have addressed the problem of meta-stability which becomes important when operating at high sampling speeds. They proposed a gray encoded ROM as the solution [12]. In the year 2006, it has been shown that the static nonlinearity presents in the track and hold circuit [13] can be reduced. In 2004, a complementary average value technique was proposed in which the input signal is pre-processed before comparing it with a fixed voltage reference level in order to simplify the comparator design [14]. In 2012 a 4-bit asynchronous binary search based ADC has been presented so as to obtain high speed applications [15].

In our proposed architecture, to reduce the area and power dissipation TMCC is introduced replacing the comparators and series combination of resistors. In addition, a standard design of encoder consisting of multiplexers, called Bit Referenced Encoder is proposed. The simulation results provide a clear message that total power consumption of the proposed Flash Type ADC reduces drastically than that of a conventional one.

3. Blocks of the Proposed ADC

3.1. TMCC: Reduction of the delay and the power consumption can be done by replacing the series combination of resistors and Comparator with TMCCs. The full form of TMCC is Threshold Modified Comparator Circuit. It is basically a buffer circuit having an inverter with modified threshold voltage followed by a NOT gate as shown in Figure 3.

In normal 2 CMOS inverter circuit the threshold voltages of two CMOS connected back to back are same but in TMCC the threshold voltage of first inverter circuit is modified every time for a specific threshold voltage or reference voltage and the second one is fixed at a particular threshold voltage. As per required reference voltage we can change the width-length ratio (W/L) of the MOS transistors used in the inverter circuit so as to get the modified threshold voltage. The relation between threshold voltage and the aspect ratio can be found from the following equation –

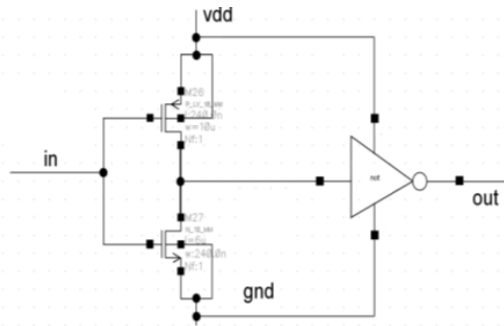


Figure 3. Circuit of the TMCC

$$V_{th} = \frac{V_{to,n} + \sqrt{\frac{1}{K_r}(V_{dd} + V_{to,p})}}{\left(1 + \frac{1}{\sqrt{K_r}}\right)} \quad (3)$$

Where,

$$K_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

$$K_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

And the transconductance ratio,

$$K_r = \left(\frac{K_n}{K_p}\right) = \frac{\mu_n \left(\frac{W}{L}\right)_n}{\mu_p \left(\frac{W}{L}\right)_p}$$

From the above equation, we can find the threshold voltage for each and every TMCC by changing the values of width and length of NMOS and PMOS separately. The following Table 1 shows different values of width and length of NMOS and PMOS to have different threshold values.

For an inverter present in TMCC when the input voltage is less than threshold (reference) voltage the pull-up transistor is ON and pull-down transistor will be OFF thereby providing a high output considered as 'Logic 1'. But when the input is higher than threshold pull-down transistor will come into ON state thereby giving a low output interpreted as 'Logic 0'. If we focus the operation phenomena of a comparator we can sense that it is quite opposite to that of a comparator. Here, in TMCC we have cascaded one NOT gate with the inverter to have the convention of a comparator. The main advantage of inclusion of NOT gate serves the purpose of logic restoration of the output of an inverter circuit.

Table 1. TMCC with Various Threshold Voltages

SLNo	TMC C	V _{TH} (Volt)	NMOS		PMOS	
			W _N (μm)	L _N (μm)	W _P (μm)	L _P (μm)
1	1st	0.225	20	0.3	0.5	10
2	2nd	0.450	12	0.3	0.5	1
3	3rd	0.675	1	0.18	0.42	0.18
4	4th	0.900	0.42	0.18	2	0.18
5	5th	1.125	0.42	1	3	0.18
6	6th	1.350	0.42	10	15	0.18
7	7th	1.575	0.42	20	30	0.18

For an inverter present in TMCC when the input voltage is less than threshold (reference) voltage the pull-up transistor is ON and pull-down transistor will be OFF thereby providing a high output considered as 'Logic 1'. But when the input is higher than threshold pull-down transistor will come into ON state thereby giving a low output

interpreted as ‘Logic 0’. If we focus the operation phenomena of a comparator we can sense that it is quite opposite to that of a comparator. Here, in TMCC we have cascaded one NOT gate with the inverter to have the convention of a comparator. The main advantage of inclusion of NOT gate serves the purpose of logic restoration of the output of an inverter circuit.

As TMCC is basically an inverter so it has a specific cut point at the voltage-transfer characteristic curve. Figure 4 shows the VTC curve of an inverter circuit. In this fig the cut point is on the middle. We need such type of comparator circuit which can compare low voltages as well as high voltages. So for that different reference voltages we should change that cut point in the VTC curve that is we should modify width-length (W/L) ratio that in turns modifies threshold voltage.

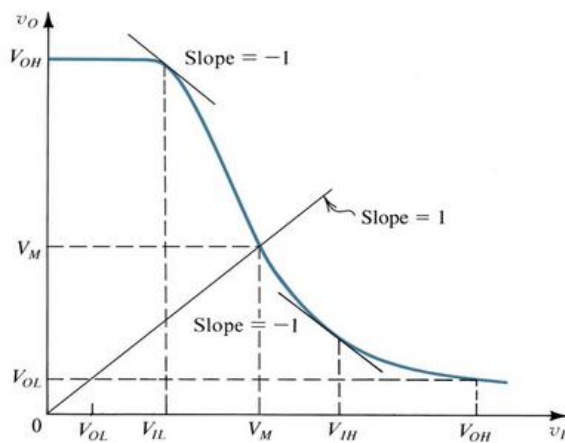


Figure 4. VTC Curve of an Inverter

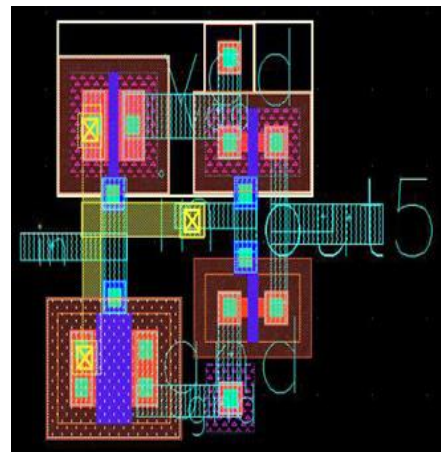


Figure 5. Layout of TMCC

3.2. Bit Reference Encoder

After the comparison of analog input voltage with different reference voltages TMCCs produce a set of data which cannot be used in their original form. To get rid of this problem encoder circuits are designed which makes those data understandable. We introduced Bit Referenced encoder circuit in our proposed ADC architecture.

Let O1, O2 O7 are the outputs from the TMCCs and D1, D2 & D3 are the final ADC outputs. The expected outputs of the proposed ADC are shown in Table 2.

Table 2. Outputs of the TMCCs and the Final ADC Output

Output of TMCC							Output of ADC		
O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	D ₁	D ₂	D ₃
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

From the above truth table we can describe the fundamental operation of our proposed Bit Referenced Encoder.

When

$O4 = 0, O6 = 0 \ \& \ O7 = 0$; Output = 000
 $O4 = 0, O6 = 0 \ \& \ O7 = 1$; Output = 001
 $O4 = 0, O6 = 1 \ \& \ O5 = 0$; Output = 010
 $O4 = 0, O6 = 1 \ \& \ O5 = 1$; Output = 011

When

$O4 = 1, O2 = 0 \ \& \ O3 = 0$; Output = 100
 $O4 = 1, O2 = 0 \ \& \ O3 = 1$; Output = 101
 $O4 = 1, O2 = 1 \ \& \ O1 = 0$; Output = 110
 $O4 = 1, O2 = 1 \ \& \ O1 = 1$; Output = 111

From the above analysis we can say that the Bit Referenced Encoder can be implemented using one 2:1 Multiplexer followed by one 4:1 Multiplexer. The block diagram of it is shown in figure 6. In this figure we have considered **out** as D3, **out_2:1** as D2, **O4** as D1.

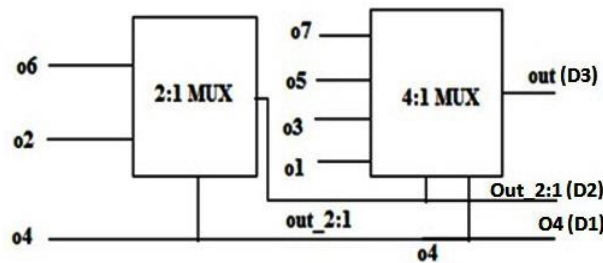


Figure 6. Block Diagram of Bit Reference Encoder

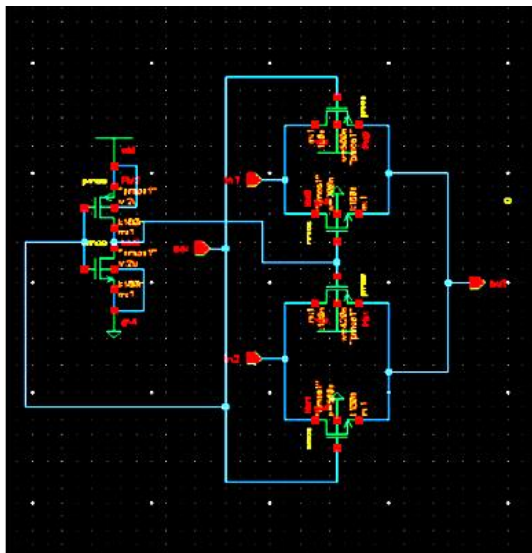


Figure 7. Schematic Diagram of 2:1 MUX using TG-CMOS

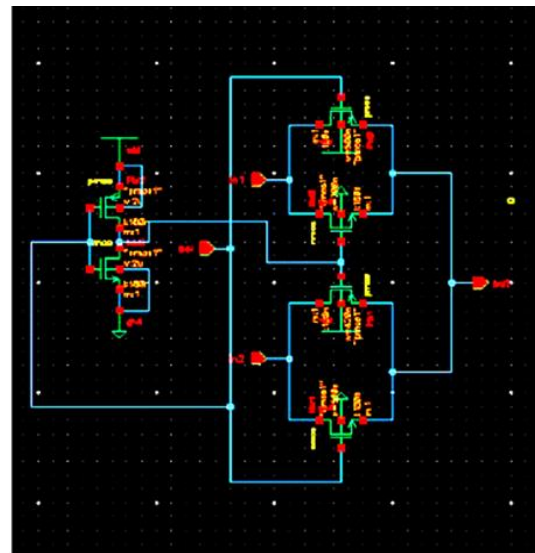


Figure 8. Schematic Diagram of 4:1 MUX using TG-CMOS

2:1 & 4:1 Multiplexers (shown in Figure 7 & 8) are designed in Transmission Gate technology so as to reduce the size of the circuit thereby reducing area and power consumption. As a result the area of the designed Bit Referenced Encoder is also reduced.

3.3 Proposed Flash Type ADC Architecture

Our proposed Flash type ADC is designed using 7TMCCs and Bit Referenced Encoder. Figure 9 shows the block diagram of our proposed Flash type ADC.

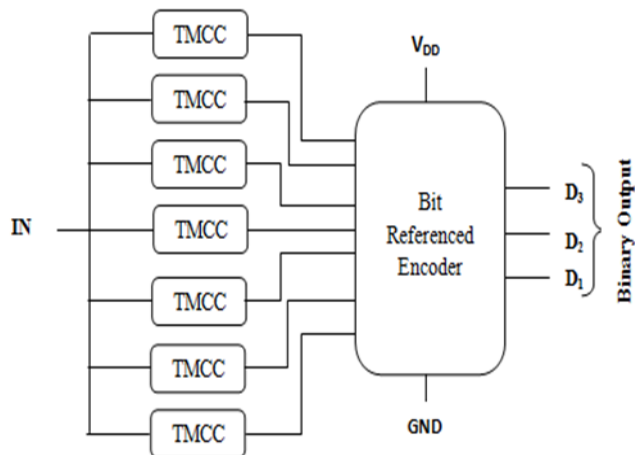


Figure 9. Block Diagram of Proposed Flash type ADC

Table 2 shows the full operation of proposed ADC and how digital bits are generated in the output of Bit Referenced Encoder. The schematic of Proposed Flash type ADC is shown in Figure 10, which is designed in CADENCE using 180 nm technologies.

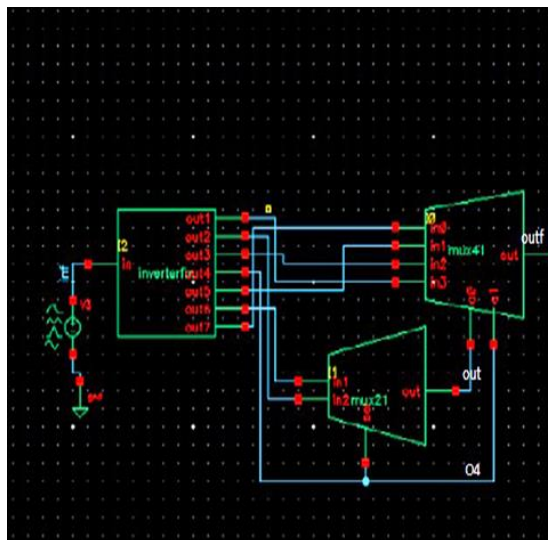


Figure 10. Schematic Diagram of Proposed Flash Type ADC

The analog input is compared with 7 different referenced voltages of TMCCs. Then the outputs are converted into digital form by the Bit Referenced Encoder. Thus an analog signal is converted into digital signal by our proposed Flash type ADC.

4. Results and Discussions:

We have designed a 3bit Flash type ADC using 7TMCCs and Bit Referenced Encoder. From table-I we see the output of ADC is producing 001,010,011,100,101,110,111. Now as we use 1.8v in cadence for our proposed ADC, we divide 1.8v into 8 different voltages

each division will be of 0.225v. Figure 11 shows the input output waveforms of our proposed ADC for a sine wave of 10MHz. when input voltage is 0.225v output of ADC produces 001 and so on. Thus input analog voltage is converted into digital form.

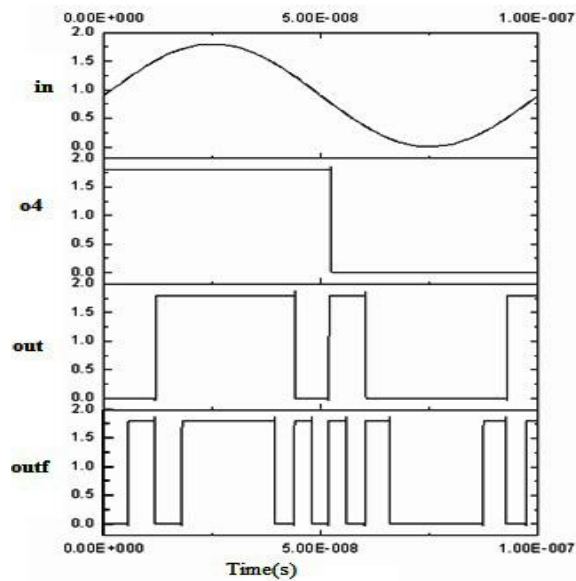


Figure 11. Input Output Waveforms of the Proposed ADC for a Sine Wave of 10MHz

A comparative analysis has been done between proposed and previously available ADCs based on some important parameter like Area and Power. The analysis gives a clear message to show that our proposed ADC is using very less area and power as compared to the other existing ADCs. Hence, the proposed method can be preferred for its simplicity in design.

Table 3 shows the comparative study of different design.

Table 3. Comparison of Different Design Styles for Low Power ADCs

Design Style	Proposed ADC	Conventional ADC	P. Kumar [18]
Architecture	Flash	Flash	Flash
Resolution	3-bit	3-bit	3-bit
Supply Voltage	1.8 V	1.8 V	1.3 V
Average Power	43.146 μ W	2397.6 μ W	36.237 mW
Area	0.0036 mm ²	0.02075 mm ²	1044um ²
Technology (nm)	180	180	180

4.2. Differential Non- Linearity and Integral Non- Linearity

Differential Non-Linearity (DNL) is the difference between the ideal and actual input code width, whereas Integral Non Linearity (INL) is the maximum deviation of the transfer function from the straight line between two points along the input-output transfer

curve. DNL indicates the deviation from the ideal 1 LSB step size of the analog input signal corresponding to a code-to-code increment. DNL, a static specification, relates to SNR, a dynamic specification. However, noise performance cannot be predicted from DNL performance, except to say that SNR tends to become worse as DNL departs from zero. INL is a measure of the straightness of the transfer function and can be greater than the differential non-linearity. The size and distribution of the DNL errors will determine the integral linearity of the converter.

Expressions for DNL and INL can be written as,

$$DNL = \frac{V_{j+1} - V_j}{V_{LSB}} - 1 \quad \text{For all } 0 < j < 2^N - 2 \quad (4)$$

$$INL = \frac{V_j - V_0}{V_{LSB}} - j \quad , \quad \text{For all } 0 < j < 2^N - 1 \quad (5)$$

Where, V_0 denotes the zero code value and V_j indicates the physical value that corresponds to the digital code 'j'.

For any gainful system DNL and INL should be zero. In DNL curve if any value goes negative, then that system will slowdown. So for a faster system DNL should not cross zero value, if crosses then that should be closer to zero value. In our proposed architecture there are five values which crosses zero value. Among them four values are in negative and one in positive. But the advantages are that those negative values are very closer to zero. In INL curve also all values should be zero or closer to zero. We achieve the INL curve having nonzero values which are very closer to zero.

Figure 12 and Figure 13 illustrate different measured DNL and INL values for the proposed ADC structure.



Figure 12. DNL Curve of Flash Type ADC using TMCC and Bit Referenced Encoder

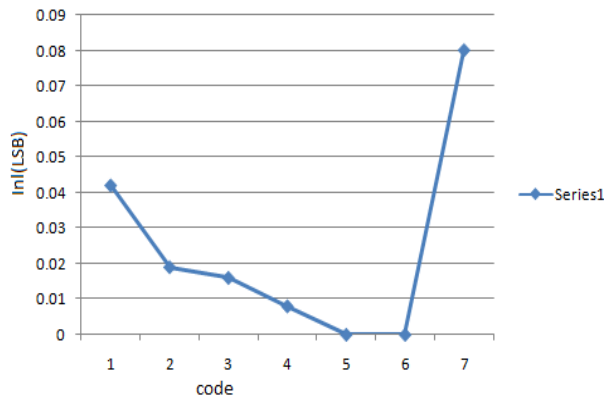


Figure 13. INL curve of Flash Type ADC using TMCC and Bit Referenced Encoder.

4.2. Missing Codes

When no value of input voltage will produce a given output code, such that the code in question never appears in the output, that code is missing from the transfer function and is known as a missing code. Any time, if DNL value is '-1' there is possibility of occurring one or more missing codes. The DNL curve of proposed ADC shown in Figure 12 gives the clear message that it is not crossing '-1' for any bit which leads to zero missing code.

Specification summary of our proposed Flash type ADC architecture are listed in Table IV for an analog sine wave of 10 MHz frequency, having input voltage of 1.8 Volt. The whole simulation job is done using CADENCE Tools and we obtain these values from different simulation run.

Table 4. Specification Summary

Values Obtained	
Parameters	Flash type ADC using TMCC and Bit Referenced Encoder
Technology	180 nm
Supply Voltage	1.8V
Average Power	43.146 μ W
Area	0.0036mm ²
Frequency	10MHz
Peak DNL	-0.16 +0.084
Peak INL	0.08
Missing Bit	Nil

Figure 14 shows the layout view of our Proposed ADC architecture done in CADENCE which occupies an active area of 0.0036 mm².

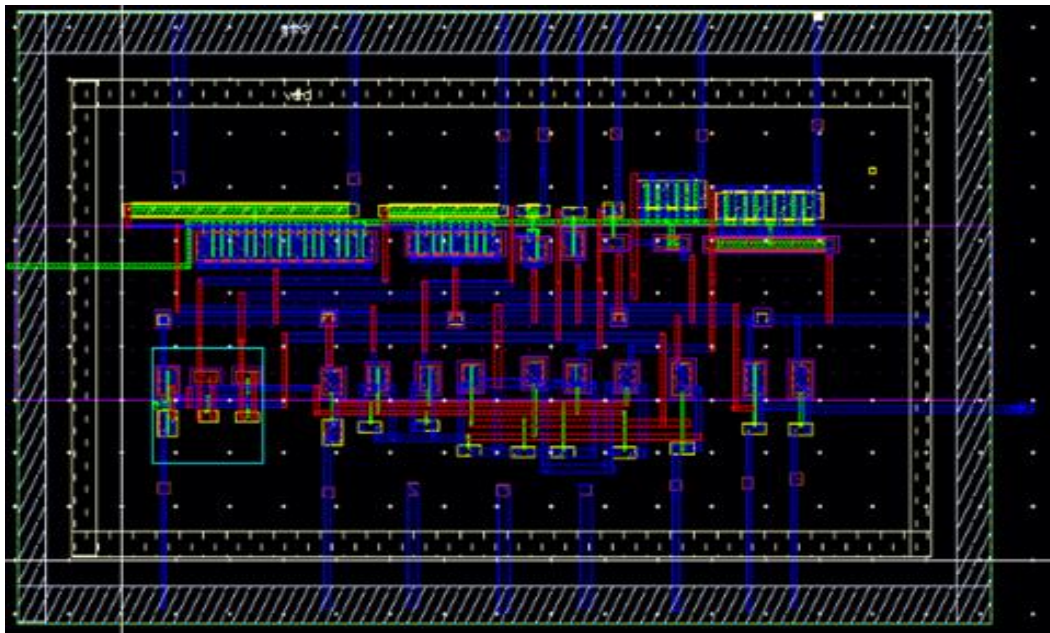


Figure 14. Layout of Proposed ADC using TMCC and Bit Referenced Encoder

4.3 Observations

After designing our proposed architecture we can observe the following points:

1. Our proposed ADC is designed with Bit Referenced Encoder which can compare low voltages as well as high voltages. Whereas conventional comparator can only compare either smaller reference voltages or else larger reference voltages.
2. Another important observation is that TMCC can be designed using 4 transistors. So it requires less chip area and power, whereas conventional comparator requires 9 transistors and so it occupies large area and consumes huge power. The comparative study of Power consumption by our proposed ADC and conventional architectures are shown by the bar chart in Figure 15.

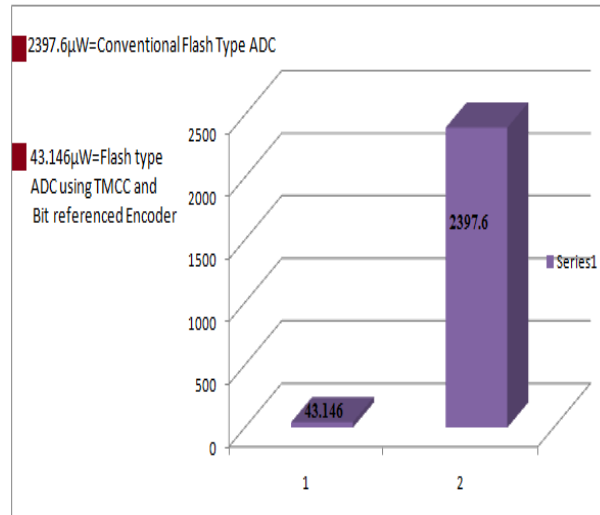


Figure 15. Comparison of Power between Conventional and Proposed ADC

5. Conclusion

Low voltage operation is one of the difficult challenges in the mixed-signal ICs. However, the minimum supply voltage for the analog circuits predicted in SIA Roadmap [44] does not follow the digital supply voltage reduction. Reducing the power requirements of existing components extends the battery life of portable devices, or allows additional functionality to be incorporated on the same power budget. Alternatively, battery size (a significant, often dominant, contribution to the size and weight of portable devices) can be reduced by decreasing the power consumption while maintaining feature set and battery life. In the proposed Bit Referenced Encoder based 3-bit Flash ADC structure, the simulation is done with the help of GPDK 180 nm technology in CADENCE. In the proposed architecture the main advantage is that the static power consumption is very low due to the absence of resistor bank. The average Power consumption is as low as 43.146 μ watt for 10 MHz input frequency. Aperture jitter, transistor matching, and increasing drain-bulk capacitance remain major problems in the development of high-speed, low-power A/D converters. But, the use of TMCC slightly reduces the transistor matching problem thereby providing a very low power high speed ADC with no missing bit. We are looking to design the same in 65 nm and 32 nm technology so as to get lesser power and lesser area based chip of ADC.

Acknowledgements

The authors would like to thank the department of ECE at Heritage Institute of Technology, Kolkata for providing CADENCE Lab to design the circuit.

References

- [1] R. van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", Boston, MA: Kluwer Academic Publishers, (2003).
- [2] R. Dennard, "Design of ion-implanted MOSFET's with very small physical dimensions", IEEE J. Solid-State Circuits, vol. 9, no. 5, (1974) October, pp. 256-268.
- [3] P. Scholtens, D. Smola and M. Vertregt, "Systematic power reduction and performance analysis of mismatch limited ADC designs", Proc. Int. Symp. Low Power Electron. Design, (2005), pp. 78-83.
- [4] B. Murmann, "A/D converter trends: power dissipation, scaling and digitally assisted architectures", Proc. IEEE Custom Integrated Circuits Conf., (2008), pp. 105-112C.
- [5] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design, Second Edition", Oxford University Press.

- [6] D. Lee, J. Yoo and K. Choi, "Design Method and Automation of Comparator Generation for Flash A/D Converter", Proceedings of the International Symposium on Quality Electronic Design (ISQED), (2002), pp. 138-142.
- [7] C. Sandner, M. Clara, A. Santner, T. Hartig and F. Kuttner, "A 6-bit 1.2GS/s Low-Power Flash ADC in 0.13 μ m Digital CMOS", IEEE Journal of Solid State Circuits, vol. 40, no. 7, (2005) July, pp. 1499-1505.
- [8] C. Donovan and M. P. Flynn, "A Digital 6-bit ADC in 0.25 μ m CMOS", IEEE Journal of Solid State Circuits, vol. 37, no. 3, (2002) March, pp. 432-437.
- [9] P. C. S. Scholtens and M. Vertregt, "A 6b 1.6 Gsample/s Flash ADC in 0.18 μ m CMOS Using Averaging Termination", IEEE Journal of Solid State Circuits, vol. 37, no. 12, (2002) December, pp. 1599-1609.
- [10] I. Mehr and D. Dalton, "A 500MSample/s, 6-bit Nyquist Rate ADC for Disk-Drive Read-Channel Applications", IEEE Journal of Solid State Circuits, vol. 34, no. 7, (1999) July, pp. 912-920.
- [11] B. S. Song, P. L. Rakers and S. F. Gillig, "A 1-V 6-bit 50MSamples/s Current-Interpolating CMOS ADC", IEEE Journal of Solid State Circuits, vol. 35, no. 4, (2000) April, pp. 647-651.
- [12] K. Uyttenhove, A. Marques and M. Steyaert, "A 6-bit 1GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction", Proceedings of the Custom Integrated Circuits Conference, (2002), pp. 249-252.
- [13] V. Srinivas, S. Pavan, A. Lachhwani and N. Sasidhar, "A Distortion Compensating Flash Analog-to-Digital Converter", IEEE Journal of Solid State Circuits, vol. 41, no. 9, (2006) September, pp. 1959-1969.
- [14] H. C. Tseng, C. Lin, H. Ou and B. Liu, "A Low-Power Rail-to-Rail 6-bit Flash ADC based on a Novel Complementary Average-Value Approach", Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), (2004), pp. 252-256.
- [15] S. Mukherjee, D. Saha, P. Mostafa, S. Chatterjee and C. K. Sarkar, "A 4-bit Asynchronous Binary Search ADC for Low Power, High Speed Applications", International Symposium on Electronic System Design, Kolkata, (2012), pp. 28-32.
- [16] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600MS/s 5.3mW asynchronous ADC in 0.13 μ m CMOS", IEEE J. Solid-State Circuits, vol. 41, no. 12, (2006) December, pp. 2669-2680.
- [17] S. Seng Wong, U.-F. Chio, C.-H. Chan, H.-L. Choi, S.-W. Sin, U. Seng-Pan and R. P. Martins, "A 4.8-bit ENOB 5-bit 500 MS/s Binary-Search ADC with Minimized Number of Comparators", IEEE Asian Solid-State Circuits Conference, (2011) November, pp. 73-76.
- [18] P. Kumar and A. Kolhe, "Design & Implementation of Low Power 3-bit Flash ADC in 0.18 μ m CMOS", International Journal of Electrical and Electronics Engineering (IJEEE), ISSN (PRINT), vol. I, no. II, (2011), pp. 2231-5284.

Authors



Aditi Kar, she was born in 4th December 1989. She received her B.E in Electronics and Telecommunication Engineering from Tripura Institute of Technology, Agartala in 2012 and M-Tech in Microelectronics & VLSI Design from Heritage Institute of Technology, Kolkata, India in May 2014. Currently, She is working as a Teaching Assistant at Tripura Institute of Technology, Agartala. Her current research interest includes Analog & Digital VLSI.



Alak Majumder, he received B.E in Electronics and Telecommunication Engineering from Tripura Institute of Technology, Agartala in 2011 and M-Tech in Microelectronics & VLSI Design from National Institute of Technology, Agartala, India in May 2013. After M-Tech he joined The ICFAI University, Tripura as a Faculty Member where he worked for 2 months. Since September'2013 he is working as an Assistant Professor in the department of ECE at National institute of Technology, Arunachal Pradesh, India. His current research interests include Analog and Digital VLSI and High Speed Interconnects. He is a Member of IEEE, IAENG and IACSIT.