

Cascaded H-Bridge with Single DC Source and Regulated Capacitor Voltage

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Abstract

Multilevel power electronic converter has wide range of applications. In multilevel power electronic converters the output can be synthesized by combining several DC voltage sources. Cascade H-Bridge multilevel inverter generally requires more number of DC sources. An alternative option is to replace all the DC sources feeding H-Bridge cells with capacitors, leaving only one H-Bridge cell with a real DC sources. But balancing the capacitor voltage is challenging. In this paper a new control method for cascade H-bridge multi level inverter fed with only one independent DC source is presented. Simulation results support the proposed control method.

Keywords: Capacitor voltage balancing, Cascaded H-bridge, H-bridge cell, Multilevel converter, Phase shift modulation

1. Introduction

In multilevel power electronic converters, the desired output can be synthesized by combining several DC sources .solar panels, fuel cells, batteries, and ultra capacitors are the most common independent sources used. These converters are having single phase and three phase applications. The first topology introduced was the series H-Bridge converter which utilized a bank of series capacitors. Later flying capacitor design. In general multilevel converters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. Applications of diode clamped multilevel converters include high-power ac motor drives in conveyors, pump, fans, and mills. But due to capacitor voltage balancing issue diode-clamped inverter has been mostly limited to 3-level. Flying capacitor involves series connection of capacitor clamped switching cells. This can be used in high-bandwidth, high-switching frequency applications such as medium voltage traction drives. Drawback of this topology is large number of capacitors are more expensive and bulky. Finally cascaded H-bridge inverter consists of series power conversion cells. Voltage and power levels may be easily scaled. Cascaded H-bridge multilevel converter has been applied to high-power and high-quality applications such as static volt-ampere reactive generation, active filters, reactive power compensators, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging. Furthermore one of the growing applications for multilevel power electronic converters is electric drive vehicles in which the traction motor is driven by batteries. The main disadvantage of this cascaded H-Bridge topology is that large number of isolated voltage requires supplying each cell. This paper has given an alternate method to overcome the disadvantage of cascaded H-Bridge multilevel inverter.

2. General Switching Methods used for Cascaded h-bridge Inverter

The method used to switch cascaded H-Bridge cells can be based either on the fundamental switching frequency that is staircase modulation, or the pulse width modulation technique. In the fundamental switching frequency approach, the switching losses are less, but the harmonic in the output voltage waveform appear at lower frequencies. Several methods are proposed in the literature to selectively eliminate harmonics in the output waveforms of multilevel converters. In the pulse width modulation switching method, the harmonic in the output waveform appear at high frequencies, but due to a higher switching frequency, the switching losses are greater.

3. Working of General Cascaded H-Bridge Inverter

The block diagram of a 5 level cascaded H-Bridge inverter system is given in Figure 1. Each H-Bridge cell was supplied by an independent DC source. The switching pattern is given in below table.

Table 1. Switching Pattern of Cascaded H-Bridge

Power devices index								Output voltages		
S ₁₁	S ₂₁	S ₃₁	S ₄₁	S ₁₂	S ₂₂	S ₃₂	S ₄₂	V _{a1}	V _{a2}	V _o
1	0	0	1	1	0	0	1	+V _{DC}	+V _{DC}	+2V _{DC}
1	1	0	0	1	0	0	1	0	+V _{DC}	+V _{DC}
1	1	0	0	1	1	0	0	0	0	0
0	0	1	1	0	1	1	0	0	-V _{DC}	-V _{DC}
0	1	1	0	0	1	1	0	-V _{DC}	-V _{DC}	-2V _{DC}

Here we are using two independent dc sources. The 5 level output voltage waveforms can be observed from Figure 2. The usage of DC source increases with the increase of output voltage level. That is for m output levels we require m-1/2 sources. This causes to increase the cost of the system.

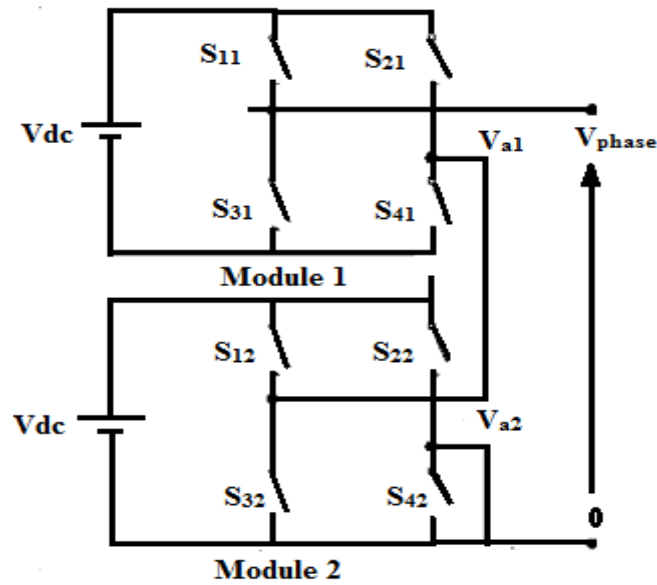


Fig 1:Block diagram of a cascaded H-bridge inverter with two independent DC sources

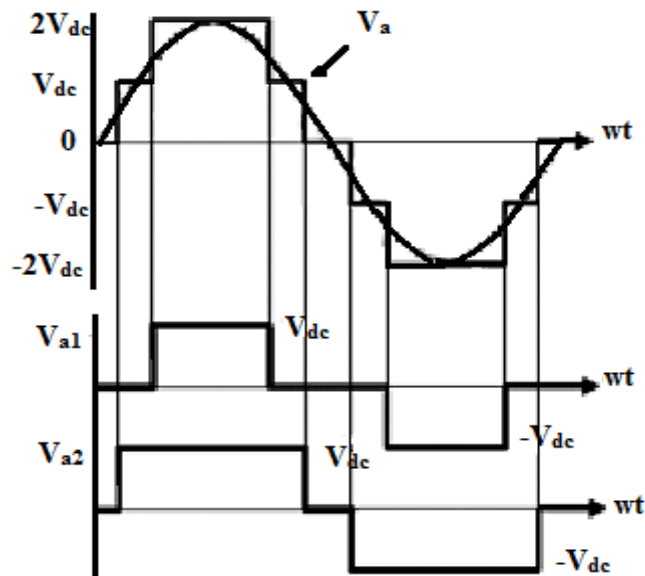


Fig 2: Output voltage waveform of a general cascaded H-bridge

To overcome the disadvantage of normal cascaded H-Bridge inverter a new topology is introduced in this paper. Here only one cell needs to be supplied by a dc power source. The remaining cells can be fed by capacitors.

4. Proposed H-Bridge Inverter

Here all dc sources feeding the H-bridge cells is replaced with capacitors leaving only one H-bridge cell with real dc voltage cell. Figure 3 shows the new cascaded inverter with only one dc source. This will yield a cost effective converter.

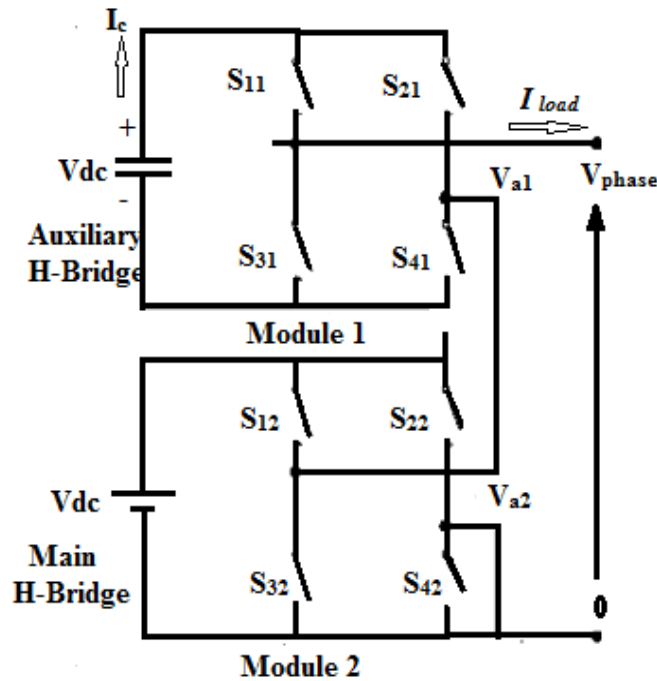


Fig 3: Cascaded H-bridge with only one DC source

However, regulating the capacitor voltage is not easy. This paper proposes a control method to single dc source H-bridge inverter to improve their capacitor voltage regulation. The proposed method phase shift modulation is robust and does not incur much computational burden. In this method the main inverter switches at the fundamental frequency, and the auxiliary inverter switches at the PWM frequency. The working theory of the cascaded H-bridge multilevel inverter is briefly introduced following sections.

5. Fundamentals of Operation

The structure of the main and auxiliary cells are similar to each other, the only difference being that the main inverter uses a dc voltage source or a battery while the auxiliary inverter uses a capacitor(see Fig 3). H-bridge cells are connected in series. Hence the output voltage is the sum of all individual cell outputs. The output voltage of the inverter can be described as

$$V_{out} = V_1 + V_2 \tag{1}$$

Most of the applications the desired output voltage waveform of the cascaded H-bridge multilevel inverter is a sinusoidal waveform that can be described as

$$V_{out,ref}(t) = V_m \sin(\omega t) \quad (2)$$

Where V_m is the desired amplitude of the output voltage.

Figure 4 describes how the desired output voltage waveform is synthesized using the main and auxiliary H-bridge cells. The main H-bridge cell, which is supplied by V_{dc} , generates a rectangle waveform (V_1). The frequency of which equals that of the desired output voltage. The width of this rectangular waveform is chosen in such way that the desired output voltage. In other words

$$\alpha = \cos^{-1}(\pi V_m / 4V_{dc})$$

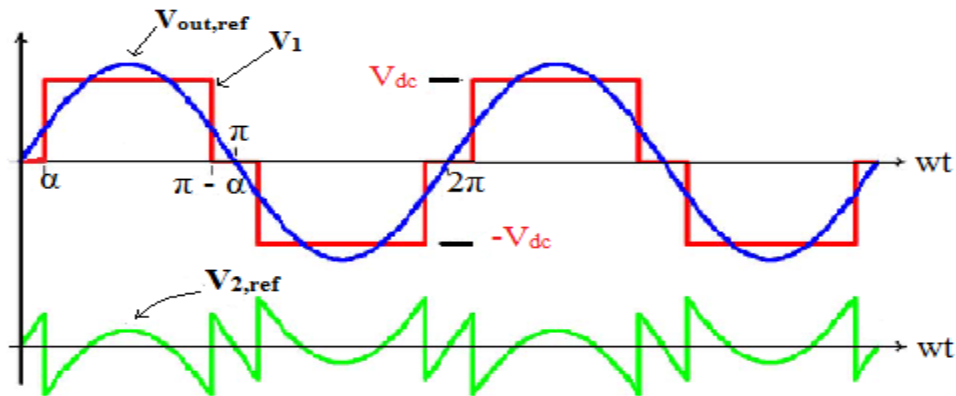


Fig 4: Generation of desired output voltage for the auxiliary bridge

Where α is the conduction angle of the main H-bridge cell. The upper trace from (Figure 4) the rectangular waveform indicates the output voltage of main H-bridge inverter. And it is compared with desired sinusoidal output of the system to generate reference voltage waveform for the auxiliary bridge. That is bottom trace in Figure 4. That part must be synthesized by the auxiliary H-bridge cell. Hence the desired output voltage can be described as

$$V_{2,ref}(t) = V_{out,ref}(t) - V_1(t) \quad (4)$$

The pulse width modulation at higher frequency will be applied to the auxiliary cell to construct $V_{2,ref}(t)$.

6. Phase Shift Modulation

Regulating the capacitor voltage in the auxiliary bridge is a challenging one. The capacitor voltage balancing is achieved by adjusting the active power that the main H-bridge cell injects into the system. By shifting the voltage waveform (Figure 5) generated by the main H-bridge cell to the left or right, one can inject more or less active power, which can be used to charge or discharge the capacitor on the auxiliary cell. Some assumptions are made to simplify the analytical description of the principle of the operation of phase shift modulation. The assumptions are

(i) The output voltage of the auxiliary cell is equal to the commanded waveform for that cell *i.e.*, $V_2(t) = V_{2ref}(t)$.

(ii) The output current is sinusoidal, as the load behaves like a low-pass filter.

The Fourier series of the rectangular output voltage waveform of the main cell can be expressed as

$$\begin{aligned} V_1(t) &= V_m \sin(\omega t) + \sum_{n=3,5} [a_n \sin(n\omega t) + b_n \cos(n\omega t)] \\ &= V_m \sin(\omega t) + h_n(n\omega t) \end{aligned} \quad (5)$$

Where $h_n(n\omega t)$ encompasses all of the harmonics in the output of the cell except for the fundamental harmonic. Based on (3), The magnitude of the fundamental harmonic of the main cell's voltage is set to be equal to the magnitude of the output voltage. The output voltage of the auxiliary bridge is given by

$$V_2(t) = -h_n(n\omega t) \quad (6)$$

In general the output current has a θ phase shift from the output voltage, *i.e.*, $i_{Load}(t) = I_m \sin(\omega t - \theta)$, the average output power can be described as

$$\langle P_{out} \rangle = 0.5 V_m I_m \cos(\theta) \quad (7)$$

The average power that the harmonics send out during a cycle is zero. Which therefore does not contribute to the output power of the cell? Thus $\langle P_1 \rangle = \langle P_{out} \rangle$, and $\langle P_2 \rangle = 0$. Now the voltage of the main cell is shifted to the right by $\Delta\alpha$ based on the operation principle of the converter, the output voltage and consequently, the output power do not change. Then the output voltage of the cells can be expressed as

$$V_1 = V_m \sin(\omega t - \Delta\alpha) + h_n(n(\omega t - \Delta\alpha)) \quad (8)$$

$$V_2(t) = V_m \sin(\omega t) - V_m \sin(\omega t - \Delta\alpha) - h_n(n(\omega t - \Delta\alpha)) \quad (9)$$

The output power of each cell is given by

$$\langle P_1 \rangle = 0.5 V_m I_m \cos(\theta - \Delta\alpha) \quad (10)$$

$$\langle P_2 \rangle = 0.5 V_m I_m [\cos(\theta) - \cos(\theta - \Delta\alpha)] \quad (11)$$

Here when $\Delta\alpha$ and θ are positive, the generated active power in the main cell will be greater than the power transferred to the load. This causes the remaining power to be delivered to the auxiliary cell, consequently charging of the capacitor cell. When $\Delta\alpha$ is positive, $\langle P_2 \rangle$ is negative, hence capacitor is charging, and when $\Delta\alpha$ is negative, $\langle P_2 \rangle$ is positive, the capacitor is discharging. Therefore controlling $\Delta\alpha$ makes it possible to charge or discharge the capacitor to regulate its voltage at the desired value. Fig 5 shows how $\langle P_2 \rangle$ changes with respect to $\Delta\alpha$. Based on this discussion a MATLAB/ simulink model has been developed.

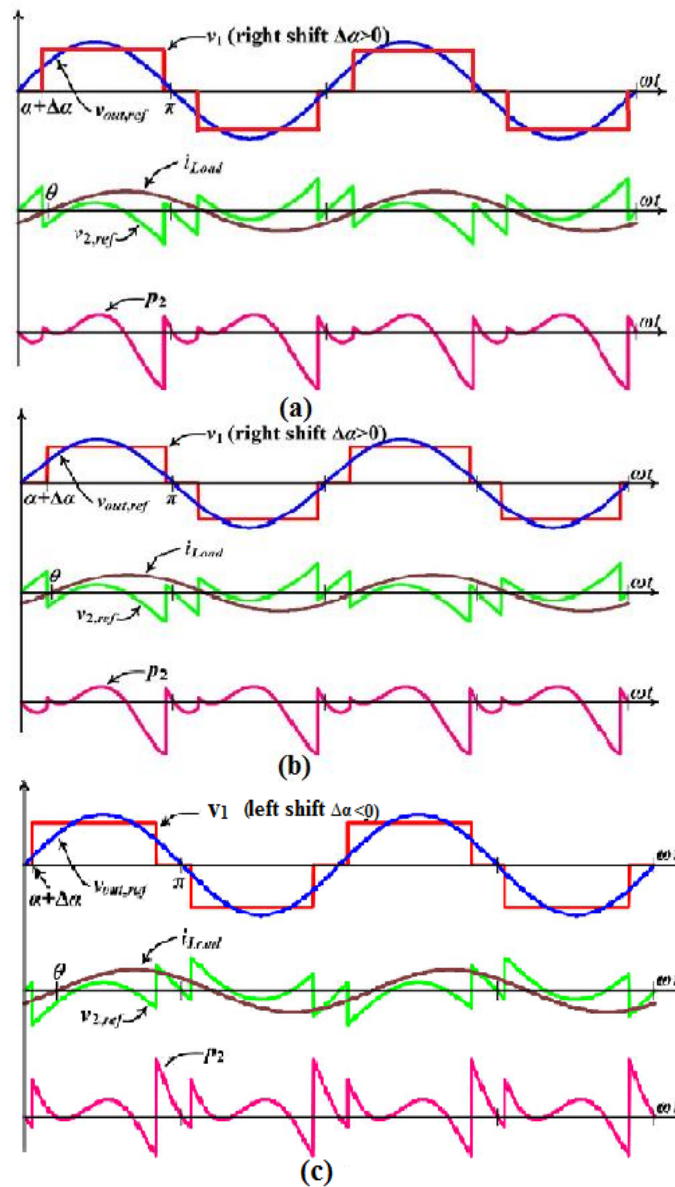


Fig 5: (a) No phase shift (b) shift to right $\langle P \rangle$ is negative capacitor charging (c) shift to left $\langle P \rangle$ is positive capacitor discharging

7. Mat lab / Simulink Model

In this model load is assumed to consist of a resistor in series with an inductor. Load comprising of a resistor with 10Ω and 15.3mH inductor connected in series. Main H-bridge voltage is 100 V and V_{dex} auxiliary bridge voltage set to 70 V . To verify the results two models has been designed. Open loop model and closed loop model. The block diagram and waveforms for open loop model is given below.

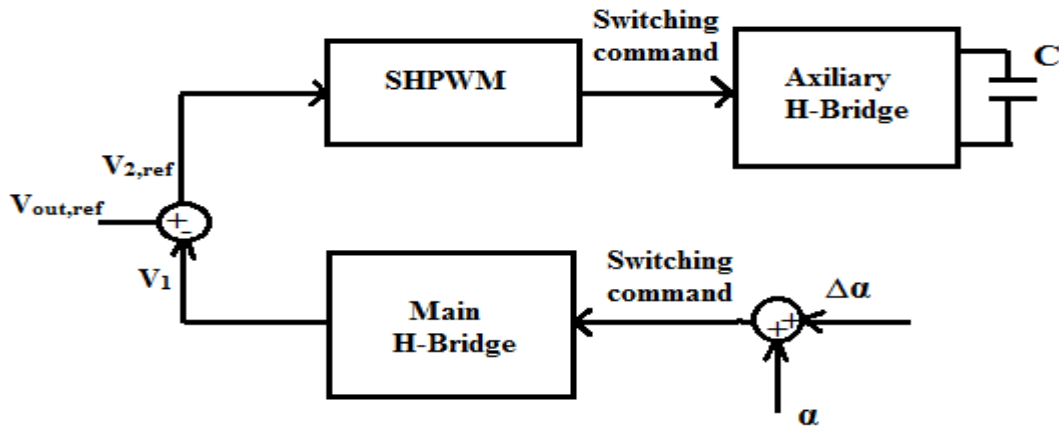


Fig 6: open loop diagram for capacitor voltage balancing

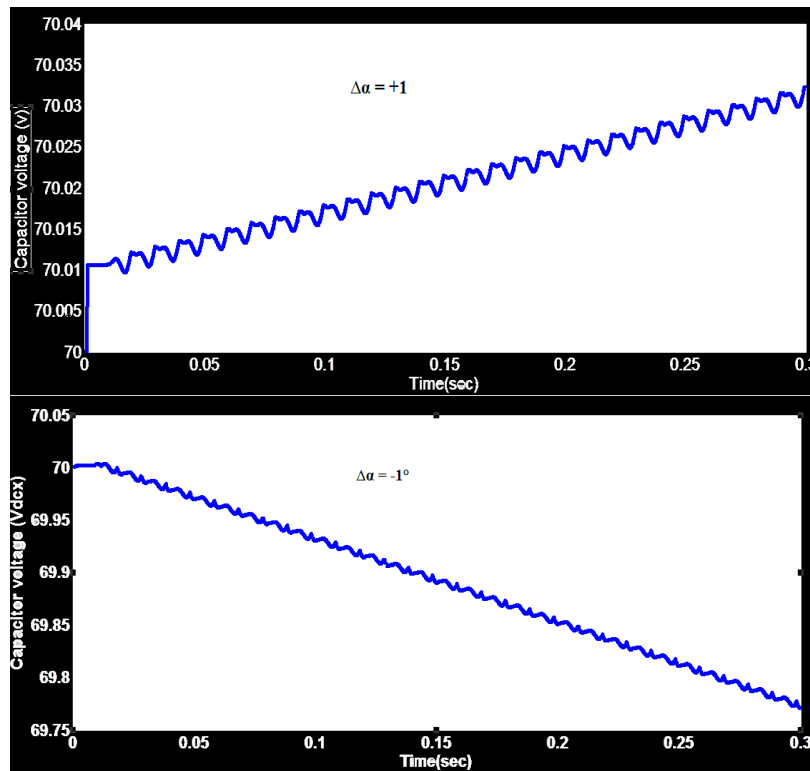


Figure 7. Simulation Results for Open Loop Phase Shift Modulation

Here as $\Delta\alpha = +1^\circ$ the capacitor voltage is increases, which indicates a charging of capacitor. When $\Delta\alpha = -1^\circ$, the capacitor voltage decreases, which indicates a discharging capacitor. Those can show in below waveforms. From above results we can observe that for α increasing capacitor is completely charging. For α decreasing capacitor completely discharging. Based on this discussion, a closed loop system for capacitor voltage regulation can be designed. The proposed capacitor voltage regulation method is shown below.

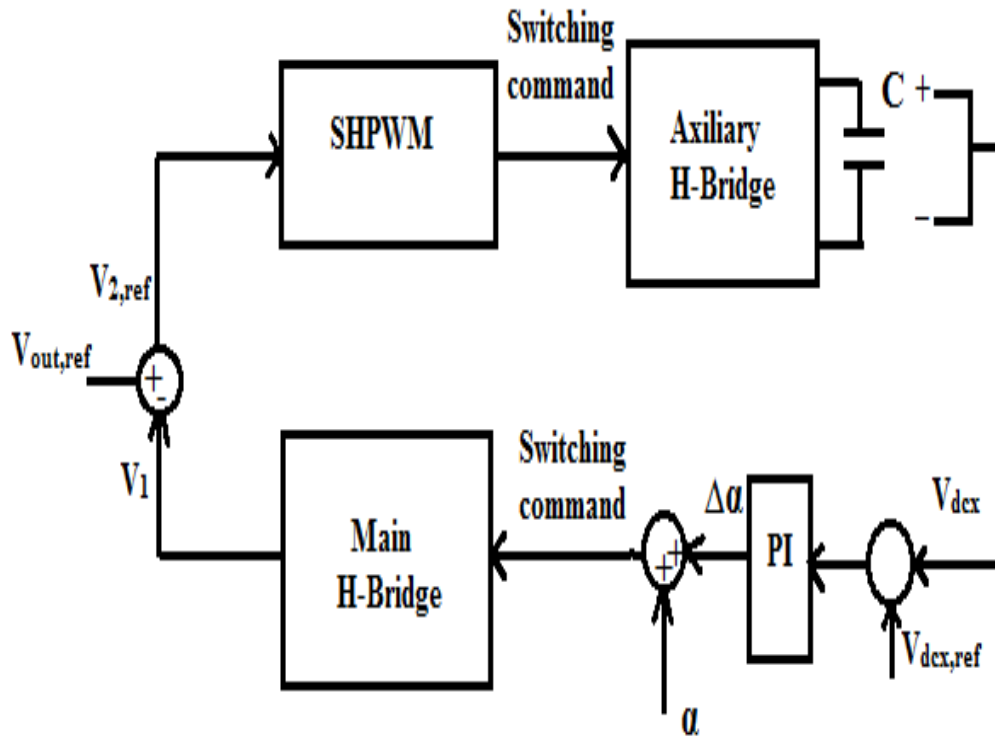


Fig 8: Closed loop control block diagram for capacitor voltage balancing system

$\Delta\alpha$ is adjusted to regulate the capacitor voltage in the auxiliary bridge. The simulation results of the closed loop phase shift system with an inductive load are given in Figure 9. Which indicates that the capacitor voltage regulation is successfully regulated the capacitor by changing $\Delta\alpha$.

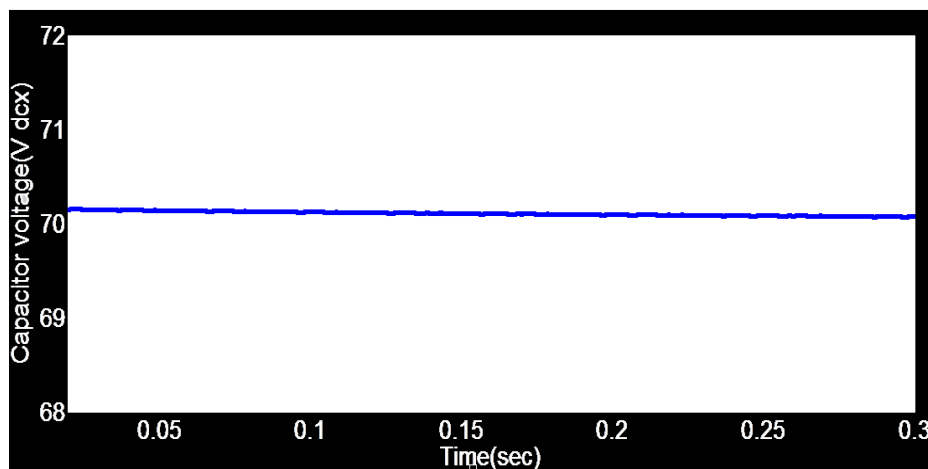
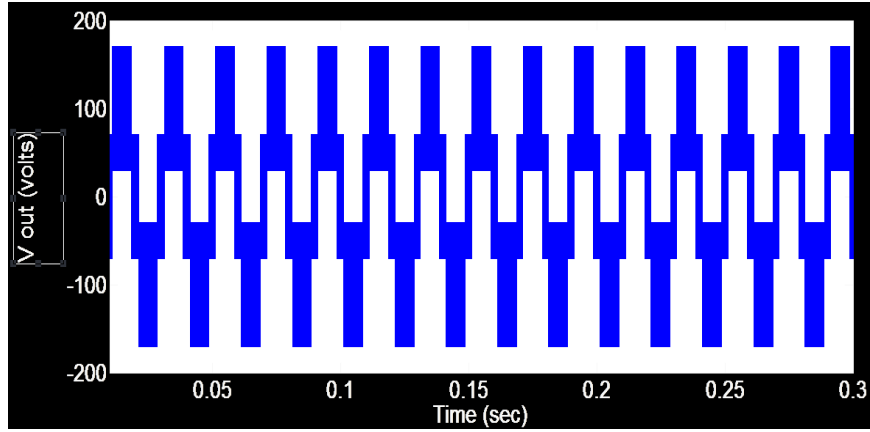
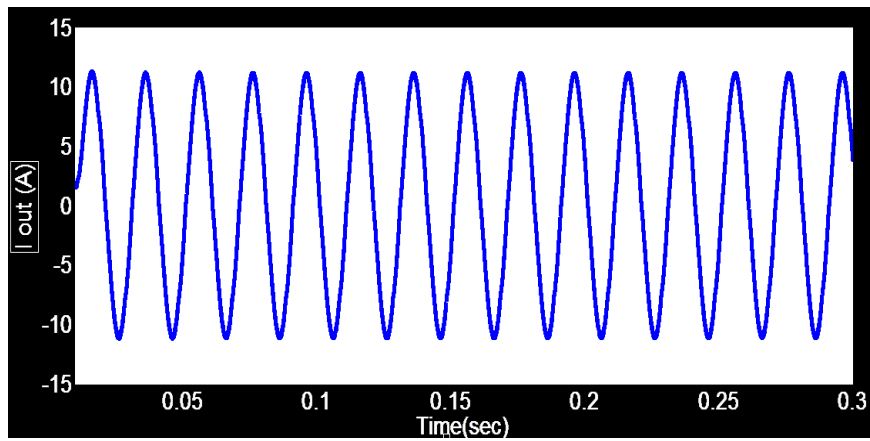


Figure 9. Regulated Capacitor Voltage



(a)



(b)

**Figure 10. (a) Closed Loop H-bridge Output Voltage
(b) Output Current**

8. Constraints on the Capacitor Voltage Selection of Auxiliary H-Bridge Cell

In this section, constraints on the voltage level chosen for the auxiliary H-bridge are discussed. The maximum value for the reference of the main H-bridge, i.e., at $\omega t = \alpha$, $\pi - \alpha$, and $2\pi - \alpha$.

It is clear that the voltage source of the auxiliary H-bridge should be chosen to be greater than the peak of its reference voltage. Based on this limitation, it is possible to find the minimum value for the voltage level of the auxiliary H-bridge.

The output voltage at α can be measured as

$$V_{\alpha-} = V_{out}(\alpha/\omega) = V_m \sin(\alpha) = V_m \sqrt{1 - \left(\frac{\pi V_m}{4V_{dc}}\right)^2} \quad (12)$$

$$V_{\alpha+} = V_{dc} - V_{out}(\alpha/\omega) = V_{dc} - V_{\alpha-} \quad (13)$$

For different values of the commanded V_m , the minimum V_{dcx} is given by

$$\text{Min. } V_{\text{dcx}} = \max (V_{\alpha-}, V_{\alpha+}) \quad (14)$$

Also modulation index is defined as

$$m = V_m / V_{\text{dc}} = 4 \cos(\alpha) / \pi \quad (15)$$

9. Conclusion

A single dc-source cascaded H-Bridge multilevel converter has been analyzed. A new control method, phase shift modulation, is used to regulate the voltage of the capacitor replacing independent dc source in the auxiliary H-bridge cell. The main H-bridge cell operates at the fundamental frequency, while the auxiliary cell runs at PWM frequency. The proposed method offers a robust regulation of the capacitor voltage when the inverter's load is inductive. Consequently at the cost of adding some minor computational burden, it leads to a more simple and cost effective single dc source multi level converter. Constraints involved in selecting the voltage source level of the auxiliary H-bridge cell also have been discussed in this paper. The experimental results show the effectiveness of the method of regulating capacitor in the auxiliary H-bridge cell.

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References

- [1] J. Rodriguez, L. Jih-Sheng and P. Fang Zheng, "Multilevel inverters: A survey of topologies, controls, and applications", *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, (2002) August, pp. 724–738.
- [2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives", *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, (2008) June, pp. 28–39.
- [3] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters", *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, (1996) May, pp. 509–517.
- [4] C. Cecati, A. Dell'Aquila, M. Liserre and V. G. Monopoli, "Design of H-bridge multilevel active rectifier for traction systems", *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, (2003) September, pp. 1541–1550.
- [5] C. Cecati, F. Ciancetta and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control", *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, (2010) December, pp. 4115–4125.
- [6] E. Ozdemir, S. Ozdemir and L. M. Tolbert, "Fundamental-frequency modulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system", *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, (2009) November, pp. 4407–4415.
- [7] H. Sepahvand, M. Khazraei, M. Ferdowsi and K. A. Corzine, "Feasibility of capacitor voltage regulation and output voltage harmonic minimization in cascaded H-bridge converters", *Proc. IEEE Appl. Power Electron. Conf. Expo.*, (2010), pp. 452–457.
- [8] E. Villanueva, P. Correa and J. Rodriguez, "Control of a single phase H-bridge multilevel inverter for grid-connected PV applications", *Proc. Power Electron. Motion Control Conf.*, (2008), pp. 451–455.
- [9] Y. Cheng and M. L. Crow, "A diode-clamped multi-level inverter for the StatCom/BESS", *Proc. IEEE Power Eng. Soc. Winter Meeting*, vol. 1, (2002), pp. 470–475.
- [10] K. A. Corzine and J. R. Baker, "Multilevel voltage-source duty-cycle modulation: Analysis and implementation", *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, (2002) October, pp. 1009–1016.

- [11] H. Sepahvand, M. Ferdowsi and K. A. Corzine, "Fault recovery strategy for hybrid cascaded H-bridge multilevel inverters", Proc. IEEE Appl. Power Electron. Conf. Expo., (2011), pp. 1629–1633.
- [12] H. Sepahvand, M. Khazraei, M. Ferdowsi and K. A. Corzine, "Startup procedure and switching losses reduction for a single-phase flying capacitor active rectifier", IEEE Trans. Ind. Electron., to be published.
- [13] M. Khazraei, H. Sepahvand, K. A. Corzine and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying capacitor multilevel power converters", IEEE Trans. Ind. Electron., vol. 59, no. 2, (2012) February, pp. 769–778.
- [14] M. Khazraei, H. Sepahvand, M. Ferdowsi and K. A. Corzine, "Hysteresis based control of a single-phase multilevel flying capacitor active rectifier", IEEE Trans. Power Electron., vol. 28, no. 1, (2013) January, pp. 154–164.
- [15] J. Dixon, J. Pereda, C. Castillo and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply", IEEE Trans. Veh. Technol., vol. 59, no. 8, (2010) October, pp. 3736–3743.
- [16] X. Kou, K. A. Corzine and Y. L. Familant, "Full binary combination schema for floating voltage source multilevel inverters", IEEE Trans. Power Electron., vol. 17, no. 6, (2002) November, pp. 891–897.
- [17] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez and J. I. Leon, "Recent advances and industrial applications of multilevel converters", IEEE Trans. Ind. Electron., vol. 57, no. 8, (2010) August, pp. 2553–2580.
- [18] J. Dixon, L. Moran, J. Rodriguez and R. Domke, "Reactive power compensation technologies: State-of-the-art review", Proc. IEEE, vol. 93, no. 12, (2005) December, pp. 2144–2164.
- [19] E. Villanueva, P. Correa, J. Rodriguez and M. Pacas, "Control of a single phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems", IEEE Trans. Ind. Electron., vol. 56, no. 11, (2009) November, pp. 4399–4406.
- [20] S. Lu, K. A. Corzine and M. Ferdowsi, "A unique ultra capacitor direct integration scheme in multilevel motor drives for large vehicle propulsion", IEEE Trans. Veh. Technol., vol. 56, no. 4, (2007) July, pp. 1506–1515.
- [21] S. Lu, K. A. Corzine and M. Ferdowsi, "A new battery/ultra capacitor energy storage system design and its motor drive integration for hybrid electric vehicles", IEEE Trans. Veh. Technol., vol. 56, no. 4, (2007) July, pp. 1516–1523.
- [22] Z. Du, L. M. Tolbert, J. N. Chiasson and B. Ozpineci, "A cascade multilevel inverter using a single dc source", Proc. IEEE Appl. Power Electron. Conf. Expo., (2006), pp. 426–430.
- [23] H. Iman-Eini, J. L. Schanen, S. Farhangi and J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers", IEEE Trans. Power Electron., vol. 23, no. 5, (2008) September, pp. 2428–2442.
- [24] Z. Du, L. M. Tolbert, B. Ozpineci and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter", IEEE Trans. Power Electron., vol. 24, no. 1, (2009) January, pp. 25–33.
- [25] M. H. Ameri and S. Farhangi, "A new simple method for capacitors voltage balancing in cascaded H-bridge SSSC", Proc. Power Electron. Drive Syst. Technol. Conf., (2010), pp. 147–151.
- [26] A. Yazdani, H. Sepahvand, M. L. Crow and M. Ferdowsi, "Fault detection and mitigation in multilevel converter STATCOMs", IEEE Trans. Ind. Electron., vol. 58, no. 4, (2011) April, pp. 1307–1315.
- [27] H. Sepahvand, M. Khazraei, M. Ferdowsi and K. A. Corzine, "A hybrid multilevel inverter with both staircase and PWM switching schemes", Proc. IEEE Energy Convers. Congr. Expo., (2010), pp. 4364–4367.
- [28] H. Sepahvand, M. Ferdowsi and K. A. Corzine, "A seven-level converter using a combination of staircase and PWM switching methods", Proc. Annu. Conf. IEEE Ind. Electron., (2010), pp. 2307–2310.
- [29] P. Kujan, M. Hromcik and M. Sebek, "Complete fast analytical solution of the optimal odd single-phase multilevel problem", IEEE Trans. Ind. Electron., vol. 57, no. 7, (2010) July, pp. 2382–2397.
- [30] B. Diong, H. Sepahvand and K. A. Corzine, "Harmonic distortion optimization of cascaded H-bridge inverters considering device voltage drops and non-integer dc voltage ratios", IEEE Trans. Ind. Electron., vol. 60, no. 8, (2013) August, pp. 3106–3114.
- [31] J. Liao, K. Wan and M. Ferdowsi, "Cascaded H-bridge multilevel inverters—A reexamination", Proc. IEEE Veh. Power Propulsion Conf., (2007), pp. 203–207.
- [32] M. D. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive applications", Proc. IEEE Appl. Power Electron. Conf. Expo., vol. 2, (1998), pp. 523–529.
- [33] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives", IEEE Trans. Ind. Appl., vol. 41, no. 2, (2005) March, pp. 655–664.
- [34] K. A. Corzine, M. W. Wielebski, F. Z. Peng and J. Wang, "Control of cascaded multilevel inverters", IEEE Trans. Power Electron., vol. 19, no. 3, (2004) May, pp. 732–738.
- [35] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla and J. M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single dc source", IEEE Trans. Ind. Electron., vol. 56, no. 7, (2009) July, pp. 2513–2521.

- [36] J. Wang, Y. Huang and F. Z. Peng, "A practical harmonics elimination method for multilevel inverters", Proc. Ind. Appl. Conf., vol. 3, (2005), pp. 1665–1670.
- [37] H. Sepahvand, J. Liao and M. Ferdowsi, "Investigation on capacitor voltage regulation in cascaded H-bridge multilevel converters with fundamental frequency switching", IEEE Trans. Ind. Electron., vol. 58, no. 11, (2011) November, pp. 5102–5111.
- [38] D. W. Hart, "Introduction to Power Electronics", Upper Saddle River, NJ: Prentice-Hall, (1997).

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