

Novel High-Efficient Full Adder Cell Based on Bootstrapped Structure

Wei Cheng^{1*} and Jianping Hu²

¹*Institute of Micro-Nano Electronic Systems, Ningbo University, Zhejiang 315211, China*

²*Faculty of Information Science and Technology, Ningbo University, Zhejiang 315211, China*

* *Chengwei20071118@163.com*

Abstract

This paper presents a comparative research of low-power and high-speed full adder cells which are based on XOR-XNOR algorithm. The adder cells are decomposed into small modules and all of them have an in-depth analysis. Several designs of each of them are implemented, optimized, simulated and analyzed separately. We also design a novel XOR-XNOR module built upon bootstrapped pass transistor logic use silicon on insulator (SOI) process with the characteristics of the full voltage swing at internal nodes and low short-circuit current which helps in reducing the power-delay product (PDP) for high performance applications. Many different full adder cells are constructed with different XOR-XNOR modules. A realistic test environment with buffers and loads are used for simulation. All full adder cells were simulated by HSPICE based on 130 nm CMOS technology at 1.2 V supply voltages. Four sets of frequencies were operated: 25 MHz, 50 MHz, 100 MHz and 200 MHz with 50% duty cycle at four different load capacitances. A comprehensive comparison and analysis are also carried out to test the performance of the adders. Each of these cells shows different performances in terms of power consumption, speed, and PDP. The simulation results of this research are expected to help designers to select the appropriate full adder cell that satisfies their specific applications.

Keywords: CMOS, Full adder, Power-delay product, Low power, Bootstrapped pass transistor logic

1. Introduction

With the explosion of mobile computers and other portable devices, low-power and low-energy design became a must. Power and energy go hand in hand, power reduction leads to lower energy consumption over a fixed time span. Arithmetic circuits are considerable contributors of power and energy in computation intensive applications and require therefore a careful power-delay design tradeoff [1-3].

Addition is a basic arithmetical operation in many VLSI systems such as DSP and microprocessor. Propagation delay, power consumption and power-delay product (PDP) are the significant quality measure parameters for most of full adder systems, and the full adder would affect the overall performance of the system. That is why optimizing the efficiency of addition is a constantly attractive research topic. The XOR-XNOR circuits are basic building blocks in various full adder cell circuits [4].

In this paper, a comprehensive approach for analyzing is presented. It is based on anatomized the adder cell into small modules, then use simulation to measure the

performance of each of them. Following this method we can find the best suitable module, then by assembling the modules together we form a fully adder circuit which will be optimized for low power.

In order to improve the comprehensive performance, the designer may make some of the tradeoffs through the circuit design styles, architecture and algorithm optimized of the adder. There are conventional implementations with different circuit styles that have been used in the past to design full-adder cells [5] and are used for comparison in this paper. Although, they all have similar function, the way of producing the internal node capacitance and the topological structure is varied. Different logic styles tend to favor one performance aspect at the expense of the others. The logic style used in logic gates basically influences the propagation time, power dissipation, and PDP.

The remainder of this paper is organized as follows. In Section 2, some low power considerations, to be taken into account when analyzing a system are reviewed. In section 3, the building modules of the full adder cell are presented,

Implemented, tested, and compared. In Section 4, we presented different full adder cells simulation results and compare these adder cells based on power consumption, speed, PDP in different test environment. Finally, performance comparisons and conclusions are presented.

2. Source of Power Consumption

There are three major components of power dissipation in CMOS circuits

1). Switching Power: Power consumed by the circuit node capacitances during transistor switching and it may be thought of as useful in that it establishes information by charging and discharging signal lines.

2). Short Circuit Power: Short energy is waste and comes from short-circuit currents which flow directly from supply voltage to the ground. The short energy represents a small percentage in the total energy consumption.

3). Static Power: Consumed due to static and leakage currents flowing while the circuit in a stable state.

The first two components are mentioned to as dynamic power. Dynamic power constitutes the majority of the power dissipated in CMOS circuits. It is the power dissipated during charging or discharging the load capacitances of a given circuit [6]. It depends on the input pattern that will either cause the transistors to switch (consume dynamic power) or not to switch (no dynamic power consumed) at every clock cycle. If the capacitance is C then the amount of charge is CV_{dd} and the current is that charge multiplied by how often the output switches. The total energy consumption (E_{total}) per cycle are expressed as

$$E_{total} = E_{dyn} + E_{leakage} \quad (1)$$

The dynamic energy consumption (E_{dyn}) is shown in equation (2).

$$E_{dyn} = V_{dd} \sum_i (C_i \times V_{dd} \times f_i) + V_{dd} \sum_i I_i \quad (2)$$

Where the summation is over each gate, and C_i is the load capacitance at the output node i . V_{dd} is source voltage. The f_i is the average rate at which the output of gate i charges and discharges. The I_i is the averages short-circuit current flowing through gate i . So we can consider how to reduce the values of these components to design circuits with low power consumption.

Estimating the power of a large circuit is a complex task. We can find the best design module through estimating the decomposed modules and then by connecting the

modules together the bigger circuit is formed, which will be optimized for low-power dissipation.

3. Full Adder Building Modules

The full adder cell can be implemented in two types of logic structures. One is static style and the other is dynamic style. Static full adders are commonly more reliable, simpler and consume less power than dynamic ones. However, dynamic adders suffer from charge sharing, high power due to high switching activity and clock load [7].

The simplest way to implement the static full-adder circuit is to take the logic equation and translate them directly into circuit. The typical full-adder function can be described as follows.

$$Sum = A \oplus B \oplus C_{in} \quad (3)$$

$$C_{out} = A(A \oplus B) + C_{in}(A \oplus B) \quad (4)$$

There are standard implementations for the full-adder cells which are used for the fundamental unit of a multi-bit adder. We may take these adders into consideration [8-10]. From the equation (3-4) we can know most adders' logic expression are based on two XOR-XNOR circuits: one to generate H (XOR) and \overline{H} (XNOR), and the other to generate the Sum output function. The C_{in} is not only used to carry-in bit but have the effect of the multiplexer.

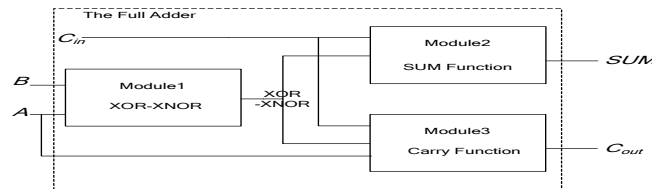


Figure 1. Building Module of Full Adder Cell

Let's rewriting equation(3-4) as

$$H = A \oplus B \quad (5)$$

$$Sum = H \oplus C_{in} \quad (6)$$

$$C_{out} = A H + C_{in} H \quad (7)$$

From the equation (5-7), it's clear that if we optimize the generation of H and \overline{H} , this can significant enhance the performance of the full adder cell. A block diagram of the full adder cell and its building block is shown in Figure 1 [11]. The module1 should be calculated H and its complement \overline{H} , which are the key variables in both equations. The module2 is needed to generate the Sum using C_{in} , H and \overline{H} . A third module is needed to generate C_{out} given H , \overline{H} , A and C_{in} . As mentioned above, the XOR-XNOR module is the critical component unit of adder cell which generates H bit and \overline{H} bit.

3.1. Circuit Analysis of Adder Cell Modules

The module1 is required to generate XOR and XNOR function. The Sum and C_{out} are generated by module 2 and module 3, respectively, which are required to provide enough

driving power to the following stage. In other words, the driving cell must provide almost full swing outputs to the driven cell. Otherwise, the performance of the circuit will be degraded seriously or become non-operative at low supply voltage. In order to optimize the performance of the full adder, it is necessary to analyze each module of a full adder in detail.

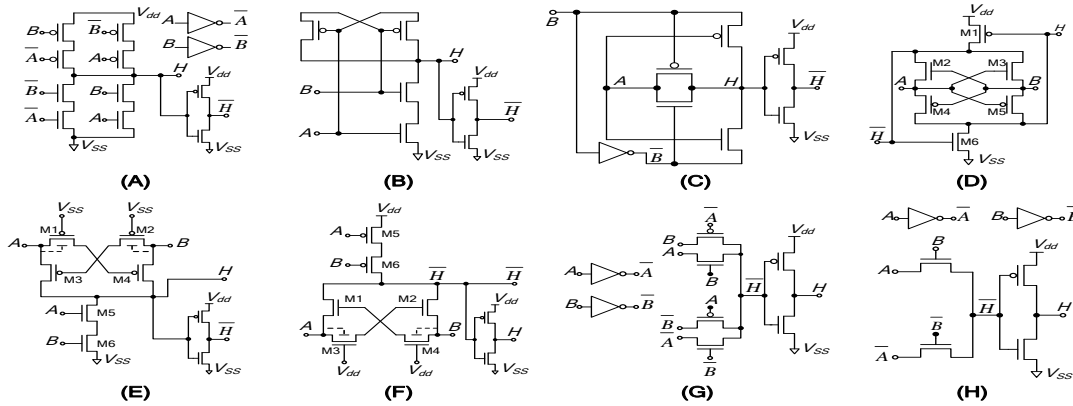


Figure 2. Different Logic Styles of the First Module (XOR and XNOR)

A. Module1: XOR-XNOR circuit

Beginning with the first module, it is required to generate both the XOR and XNOR functions. The XNOR function can be realized by XOR function with an inverter. Another method is to use both of the XOR and XNOR modules to generate the XOR-XNOR function, but it need more transistors and more power will be dissipated. Several different logic styles have been proposed to implement both the XOR-XNOR functions are shown in Figure 2. A minimum of six transistors are presented in Figure 2, while the module with more than 14 transistors will not be competitive because of the large power consumption.

In the following paragraphs, the characteristic of first module which are presented will be briefly described as follows.

(1). Complementary CMOS Logic

Figure (2A) uses complementary CMOS structure (pull-up &down networks) has eight transistors and involves minimum design risk. One of the advantages of the complementary CMOS cell is high noise margins and stable operation at low voltages. The layout of CMOS gates is symmetrical due to the complementary transistor style. The disadvantages of cell is the large number of PMOS which results in significant area overhead, more power consumption and high input loads, what's more, the high input capacitance produces an unwanted additional delay.

(2). Pass Transistor Logic (PTL)

Figure (2B) and Figure (2H) use Pass-Transistor Logic (PTL) has six transistors and eight transistors include the inverters which are needed to create the complement of A and B, respectively. The Figure (2B) uses single pass transistor logic which uses nearly half as many transistors and has an incomplete voltage swing at the output nodes, so the dynamic power consumption is reduced and the propagation delay is affected. It is not suitable in all applications due to a weak drivability at the output for $A = B = 0$. Furthermore, it's not operation well below 1.2V supply voltages for low power application; Figure (2H) uses complementary pass transistor logic to realize an XOR-XNOR function. However, the

outputs of the nMOSFET pass-transistor network suffer from threshold voltage drop, which results in the incomplete turn-off of pMOSFET's in the inverters. It can be suffered from large power consumption and also leads to performance degradation and severe design limitations. This structure could require buffer to achieve desirable outputs. One drawback of the CPL logic is the current-driving capability which is limited and delay increases with long pass structure chains, so buffering is needed to restore the transmitted signal and improve the driving capability [12-14]. However, it can be suffered from large power consumption due to short circuit current between the power supply and ground from inverters,

(3). Double Pass-Transistor Logic (DPL)

Figure (2G) has 10 transistors include two inverters uses double Pass-transistor logic in which both NMOS and PMOS logic network are used [15]. The advantages of this gate avoids the nMOSFET threshold voltage drop issue of the CPL design and eliminate the static power consumption, The problems of narrow noise margin and performance degradation at low supply voltages, which occur in CPL circuits due to the threshold voltage drop, are avoided. However, the drawback of this gate is a large area and input capacitances because of the PMOS used [16].

(4). Transmission Gate Logic

Figure (2C) has eight transistors which use one inverter, one transmission gate and two pass transistors to produce a XOR circuit, and then the XNOR function is implemented by using an inverter. Although it keeps full swing operation, the circuit consumes more static power due to the inverter and bigger transistor count.

(5). Complementary cross-coupled structure

Figure (2D) uses the complementary cross-coupled structure to produce the XOR and XNOR functions. It is able to provide full voltage swing at the output nodes because of the effect of two feedback transistors (transistors M1 and M6), which will lower the maximal operating frequency and require the MOSFETs to be rationed. The propagation delay may be suffered a small increase when the feedback transistors try to recover the threshold voltage loss. The case can be illustrated as follows: consider the case when $A = 1$ and $B = 1$, NMOS transistor M2 will charge the output \overline{H} towards 1. However, since a NMOS transistor passes only a weak '1', the output \overline{H} will be charged only to $V_{dd}-V_m$, the $V_{dd}-V_m$ at the \overline{H} output node will drive NMOS transistor M6 to fully discharge the H to 0, which, in turn, will drive PMOS transistor M1 to charge the output \overline{H} to a strong '1'. Thus for $A = 1$ and $B = 1$, the \overline{H} output node generated a fully '1' without a threshold voltage loss problem. However, when the supply voltage is below $2|V_{tp}|$ and the $V_{dd}-V_m$ cannot turn on the NMOS transistor, the feedback circuitry is not effective in restoring the output voltages to their full logic states.

As mentioned above it may be noted that the cell can easily be used for low power operation when the supply voltage is scaled down (as long as it keeps above $2|V_{tp}|$).

(6). Bootstrapped pass transistor logic

Figure (2E) and Figure (2F) which use the bootstrapped pass transistor logic to produce the XOR-XNOR functions on silicon on insulator (SOI) for low power design is presented in this paper. The use of bootstrapped pass transistor logic has been overcome the issue of output voltage loss which causes increase in short circuit current and degradation of the driving power. The principle of bootstrap effect experienced by coupling capacitance between source and gate, and the drain voltage of NMOS pass-transistor is able to rise up to V_{dd} without using pull-up PMOS by boosting the gate voltage higher than V_{dd} . The principle of bootstrapped

pass transistor logic is shown in Figure 3. The transistor M1 is for signal propagation and transistor M2 on silicon on insulator (SOI), called “isolation transistor,” is able to control the threshold voltage (V_{th}) only by changing body voltage without increase in leakage power. It’s effective to improve both speed and driving power. When the source signal begin to rise, through the coupling effect of C_{gs} and the parasitic capacitance (C_{par}), the gate voltage of transistor M3 (V_{gate}) rises up higher than V_{dd} .

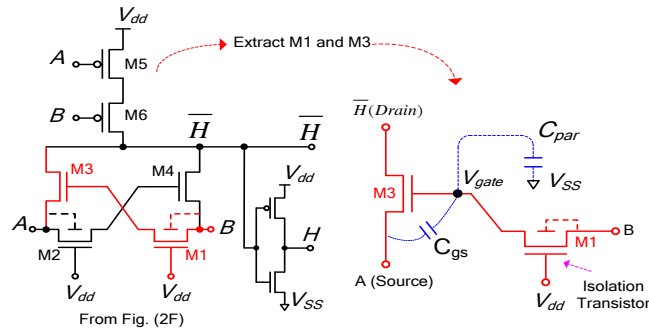


Figure 3. Principle of Bootstrapped Pass Transistor Logic

The detailed process of bootstrap can be illustrated as follows:

1. When $A=0$ and $B=1$, the V_{gate} is actually able to rise only up to $V_{dd} - V_{m}$.
2. If signal A now changes from 0 to 1, the A increased by ΔA and the V_{gate} increased by ΔV_{gate} . The value of V_{gate} is decided by the value of C_{gs} and C_{par} are as shown in equation (8):

$$\Delta V_{gate} = \frac{C_{gs}}{C_{gs} + C_{par}} \times \Delta A \tag{8}$$

Add the previous value, the $V_{gate} = \Delta V_{gate} + V_{dd} - V_{m}$ (9)

Now the V_{gate} is easily higher than $V_{dd} + V_{m}$, and then the \bar{H} have a fully swing voltage. The output waveform of Figure (2F) is shown in Figure 4. By similar arguments it can be seen that for Figure (2E) XOR-XNOR gate.

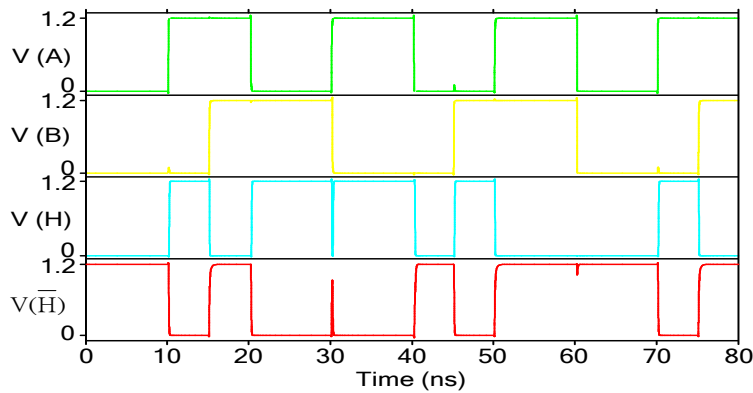


Figure 4. Output Waveform of Bootstrapped Pass Transistor Logic XOR-XNOR Gate

Simulation results: After discussion the characteristic of the XOR-XNOR cell as illustrated above, the results of the simulation at 100MHz input frequency and 20fF load capacitance are summarized in Table 1.

Table 1. Simulation Results of First Module

TYPE	Delay (ns)	Power (μ w)	PDP (fJ)
A	0.1433	3.7816	0.5419
B	0.1805	2.0815	0.3757
C	0.1167	2.4019	0.2803
D	0.1219	4.2997	0.5241
E	0.1295	2.2218	0.2877
F	0.1069	2.1841	0.2335
G	0.1213	3.2268	0.3914
H	0.1938	2.5396	0.4922

From Table 1 the Figure (2B) has consumed less power than Figure (2C) due to the incomplete voltage swing, but the delay is the second largest because of the weak current-driving capability. So, it's not suitable for VLSI when the supply voltage is low. The Figure (2F) is the best design with the lowest PDP values. As a result, it dictates that the Figure (2F) uses the bootstrapped pass transistor logic may be the most suitable first module for adder cell.

B. Module2: Sum circuit

This module can be realized by XOR-XNOR function. An important requirement of second module is to provide enough driving capability to the following circuits. In [17], it presents four different designs of second module. We choose the one which use the transmission gate logic to implement the XOR-XNOR function as shown in Figure 5 for this paper.

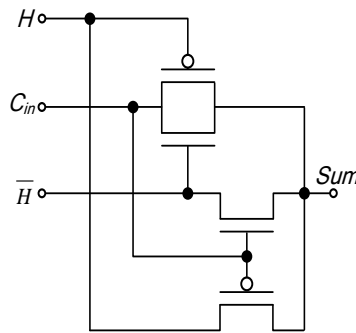


Figure 5. One Suitable Design of the Second Module

C. Module3: C_{out} circuit

The third module is required to produce the carry output which can be realized by XOR-XNOR function [17]. The Figure 6 uses transmission gate logic with four transistors have a fully voltage swing and can generate present output C_{out} .

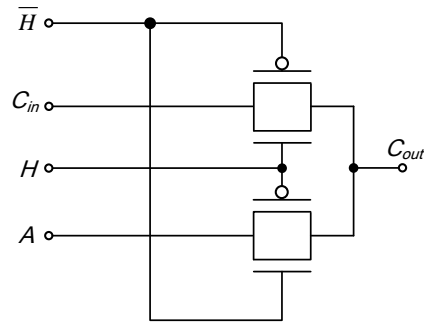


Figure 6. Best Suitable Design of the Third Module

4. Simulation of Full Adder Cells

A full adder can be built by connecting three modules together. In this section, it introduces eight different 1-bit adder cells for the purpose of analysis and comparison. The cells are shown in Figure 7 at the last page of this paper.

4.1. Simulation Environment Setup

All the circuits are designed in Cadence VIRTUOSO environment using CMOS design kit. The netlists of all adders are extracted and simulations are carried out at 27 °C with an input frequency of 25 MHz, 50 MHz, 100 MHz, and 200 MHz, respectively. By optimizing the transistor size of all adders considered, the Power-delay product (PDP) can be set to achieve minimum as far as possible.

We use six input patterns to cover all test situations. Each model is simulated 4 times using frequencies at 25 MHz, 50 MHz, 100 MHz, and 200 MHz. Four different output loads of 0fF, 10fF, 20fF and 40fF are used for power and delay measurements. Thus, for each adder, 96 HSPICE simulations runs (4 frequencies * 6 patterns * 4 frequencies) are execute. This present a total of 768 simulation runs are comparison (96 simulations/adder * 8 adder cells).

For a simulation, 50 complete periods are given. The average power of every adder is taken from the beginning of the second period to the end of the fiftieth period. In order to avoid transient glitches, the testing can not include the first period.

In this paper, the time-delay is defined as the maximum delay which is associated with the longest path is measure for SUM and C_{out} output in the circuit, the value of time-delay has been measured from 50% of voltage level of input signals (after the buffers) to the 50% of voltage level of output signal, the Power-delay product (PDP) is the significant quality measure parameter of the efficiency and a compromise between power dissipation and speed for CMOS circuits [18]. This value is calculated from worst-case delay multiplied with average power consumption is given as equation (24).

$$PDP = Power_{average} \times Delay_{worst-case} \quad (10)$$

To produce more realistic performance in the simulation, buffers are added to all the three inputs nodes. The complete simulation environment is shown in Figure 8. The circuit signals are probed at the outputs and at the inputs of the output inverters [19]. The cell was simulated by HSPICE based on 130 nm CMOS technology at 1.2V supply voltages.

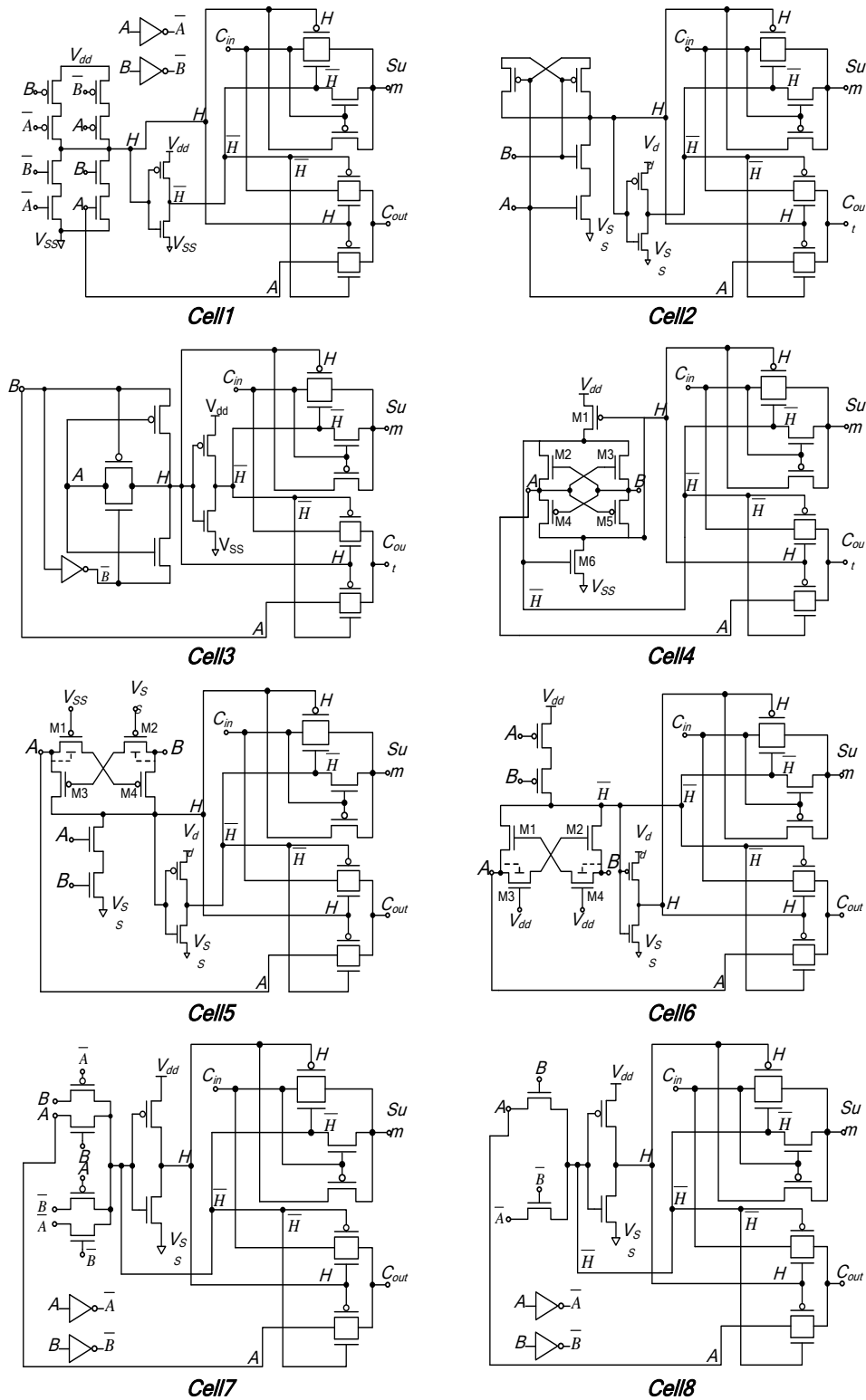


Figure 7. Eight 1-bit Full Adder Cells

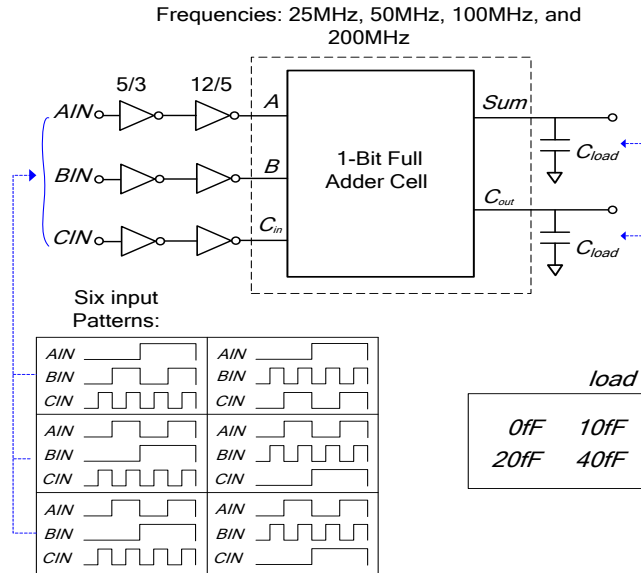


Figure 8. Simulation Environment

4.2. Simulation Results and Comparison

We compared the performance of eight full adder cells, and the simulation results for different cells are summarized in Figure 10 and Figure 12. It shows the values for the full-adder's performance comparison regarding propagation delay, average power dissipation and PDP.

Figure (10A), Figure (10B), Figure (10C), and Figure (10D) show the propagation delay and power measurement for loads of 0fF, 10fF, 20fF, and 40fF, respectively. Regarding propagation delay, from the Figure we can see that the maximum propagation delay of all cells increased as load capacitance increases, it's demonstrated by the simulation results here. Those show the cell8 and cell2 have larger delay than the rest of analyzed cells at four different load capacitance, it's due to using pass transistor logic at the first module which produces a non full swing intermediate signal and has poor output driving capacitance. The cell6 has the lowest delay in the entire adder cells simulated here and the propagation delay at four different frequencies is almost equal.

Considering power dissipation, it's clear that cells with the same number of transistors produce different power consumption values. From Figure 10, it's indicated that, as frequency is increased, the power dissipation increases. It also shows that the best cell which consumes the least power is *Cell6*, although it does not have the least transistor count. Its schematic and layout are shown in Figure 11. It uses the bootstrapped pass transistor logic with SOI MOSFET for improvement in both speed and power consumption. The *Cell6* consumes approximately 8% to 35% less power than seven other full adder cells at four different frequencies and four different loads. The *Cell3* which is based on the transmission gate logic comes second. The *Cell4* which has two feedback transistors in the first module consumes the largest power dissipation than all other cells due to the short-circuit path from V_{dd} to V_{SS} when simulated in a more realistic environment. This can be illustrated as follows: consider input pattern of $A=B=0$ (generally these signals are fed from inverters) applied to the gate. If B now changes from 0 to 1 an instantaneously short-circuit path from V_{dd} to V_{SS} arise, as shown in Figure 9 [20].

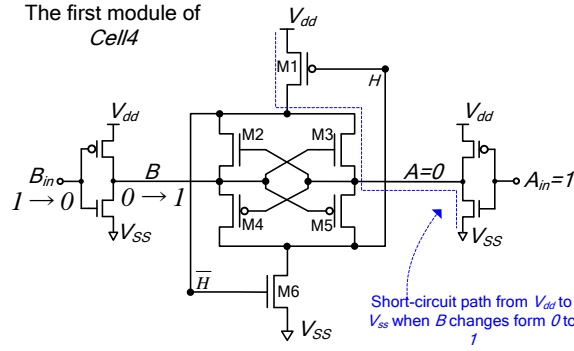


Figure 9. Short-Circuit Path of the Module 1 of Cell 4

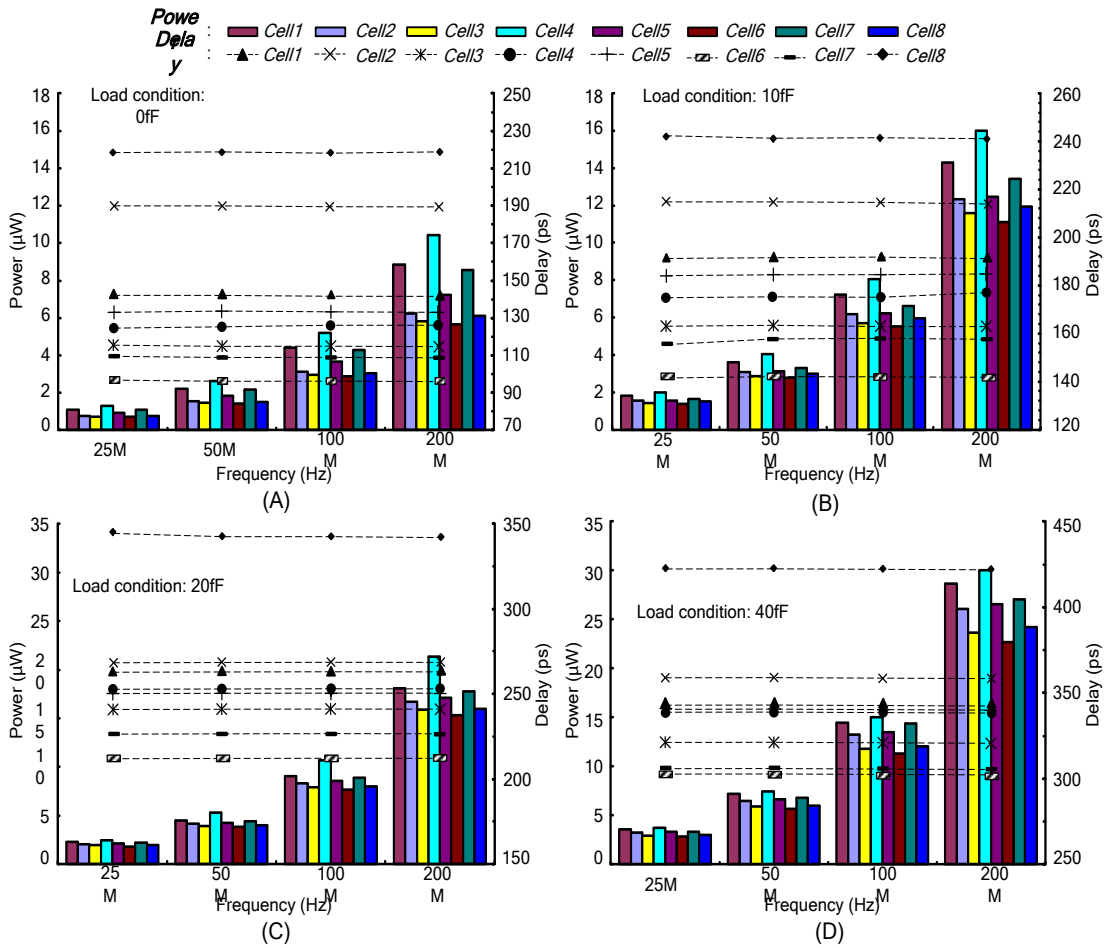


Figure 10. (A) Variation of Power and Delay with Input Frequency at the Load of 0fF

(B) Variation of Power and Delay with Input Frequency at the Load of 10fF

(C) Variation of Power and Delay with Input Frequency at the Load of 20fF

(D) Variation of Power and Delay with Input Frequency at the Load of 40fF

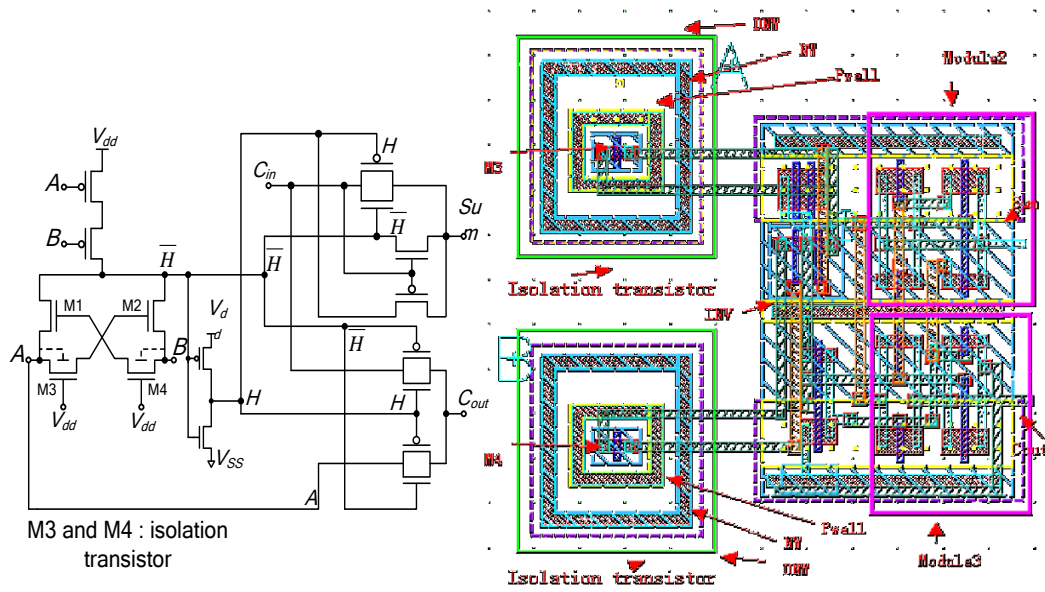


Figure 11. Schematic of Cell 6 and its Corresponding Layout which used Deepwell Technology

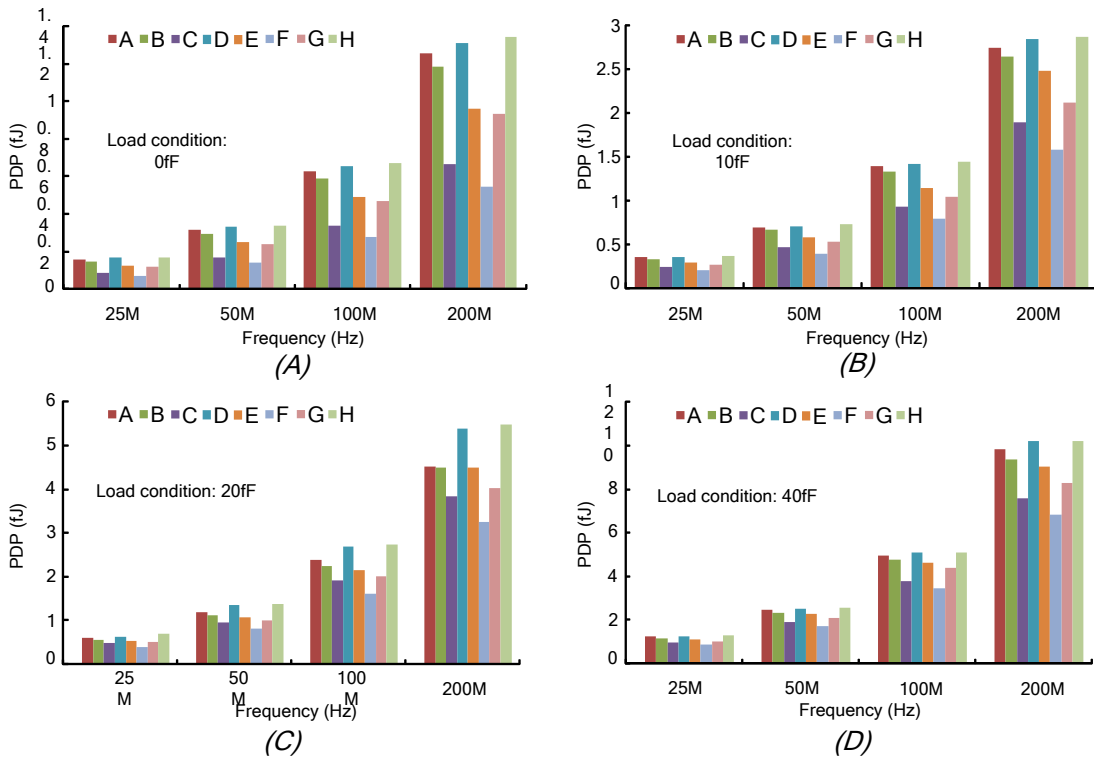


Figure 12. (A) Variation of PDP with Input Frequency at the Load of 0fF. (B) Variation of PDP with Input Frequency at the Load of 10fF. (C) Variation of PDP with Input Frequency at the Load of 20fF. (D) Variation of PDP with Input Frequency at the Load of 40fF

The PDP is always a quantitative measure of the performance of the trade-off between power consumption and propagation delay, and is significantly important when low-power operation is needed. The results of simulation under different frequencies and loads are shown in Figure 12. From the simulation results it can be observed that the *Cell6* (Novel circuit) has the best performance and takes approximately 5% to 45% less than all others under the four different frequencies at the load of 0fF, while for the load of 40fF it becomes higher by 3% to 17%.

Overall, the *Cell6* (Novel circuit) which has bootstrapped pass transistor logic use silicon on insulator (SOI) process is an excellent alternative in this paper for PDP-efficient designs, and the simulation results of this research are expected to help designers to select the appropriate full adder cell that satisfies their specific applications.

5. Conclusion

In this paper, the simulation results shows that the *Cell6* (Novel circuit) which has bootstrapped pass transistor logic use silicon on insulator (SOI) process outperforms the other adders analyzed by reducing the power consumption and delay,

The comprehensive simulation shows that PDP of the *Cell6* circuit is improved up to 5%-45% as compared with all other reference adder cells at the load of 0fF, while for the load of 40fF it becomes higher by 3% to 17%. The experimental results confirm that the *Cell6* is novel and efficient for system applications.

References

- [1] Matsuzawa, "Low-voltage and low-power circuit design for mixed analog/digital systems in portable equipment", IEEE J. Solid-State Circuits, vol. 29, (1994) April, pp. 470-486.
- [2] A. Chandrakasan and R. Brodersen, "Minimizing power consumption in digital CMOS circuits", Proc. IEEE, vol. 83, (1995) April, pp. 498-523.
- [3] N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", (3rd Edition).
- [4] S. Wairya, G. Singh, R. Vishant, K. Nagaria and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder cell", IEEE Proc. International Conference on Current Trends in Technology (NUiCONE), Ahmedabad, India, (2011) December, pp. 1-7.
- [5] S. Kajihara and T. Sasao, "On the adders with minimum tests", Test. Symposium, (1997) November, pp. 10-15.
- [6] H. Lee and G. Sobelman, "A New Low-Voltage Full Adder Circuit", IEEE Int. Symp, on Circuits and Systems, (1997) March, pp. 88-92.
- [7] M. Hosseinghadiry, H. Mohammadi and M. Nadisenejani, "Two new low power high performance full adders with minimum gates", IEEE trans., circuit and system, (2009), pp. 124-130.
- [8] A. M. Shams and M. A. Bayoumi, "A structured approach for designing low power adders", Computers. Signals. Systems & amp, vol. 1, (1997) November, pp. 757-761.
- [9] J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital integrated circuits, a design perspective", Prentice-Hall. Inc, (1996).
- [10] V. Pudi and K. Sridharan, "Low Complexity Design of Ripple Carry and Brent-Kung Adders in QCA", IEEE trans. Nanotechnology, vol. 11, (2012) January, pp. 105-1190.
- [11] A. Weinberger and J. L. Smith, "Logic for high speed addition", Nat. Bur. Stand. Circ., (1958), pp. 3-12.
- [12] S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw Hill Publication, New Delhi, (2003).
- [13] J. P. Uyemura, "Circuit Design for CMOS VLSI", Kluwer Academic Publishers, (1992).
- [14] K. H. Cheng and C. S. Hang, "The Novel Efficient Design of XOR/XNOR Function for Adder applications," Proceeding of the 6th IEEE International Conference on Electronics, Circuits and Systems, ICECS'99, vol. 1, (1999) September, pp. 29-32.
- [15] A. Sudsakom, S. Tooprakai and K. Dejhan, "Low power CMOS full adder cells", ECTICON, (2012) May, pp. 1-4.
- [16] P. Y. K. Cheung, *et al.*, "High speed arithmetic design using CPL and DPL logic," Proceedings of the 23rd European Solid-State Circuits Conference, (1997) September, pp. 360-363.

- [17] A. M. Shams and M. A. Bayoumi, "A structured approach for designing low-power adders," Proc. 31st Asilomar Conf. Signals, Systems Computers, vol. 1, (1997) November, pp. 757-761.
- [18] K. Dongho and T. Ambler, "Low power carry-lookahead adder by using dependency between generation and propagation," in Proc. IEEE Devices, Circuits and Systems, pp. C68/1-C68/6, (2000) March.
- [19] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," IEEE T. on VLSI Systems, vol. 19, (2011) April, pp. 718-721.
- [20] D. Radhakrishnan, "Low-Voltage Low-Power CMOS Full Adder," IEEE Proceedings on Circuits Devices and Systems, vol. 148, no. 1, (2001) February, pp. 19-24.

Authors



Wei Cheng, he is a graduate student - Ningbo University. His research interests include Computer Networks, and low-power integrated circuits design.