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Microwave Analysis for Intrinsic and Extrinsic Characteristics of AlGaN/GaN pHEMT

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Abstract

In this paper, a simple non-linear analytical charge control model for the DC and microwave characteristics of AlGaN/GaN MODFET is presented. The effect of parasitic resistances R_s and R_d is also incorporated. The model has also been extended to obtain the expressions for transconductance, drain conductance and cut-off frequency of the device. The model predicts a high transconductance of 502.6mA/mm at 1Vof gate bias and a maximum cut-off frequency of 22.5GHz for a 50nm device gate length, which is important in realizing the device for microwave applications. The extrinsic and intrinsic characteristics show close agreement with the published results proving the validity of the model.

Key-words: *AlGaN/GaN MODFET, parasitic resistances, extrinsic and intrinsic characteristics*

1. Introduction

High Electron Mobility Transistor (HEMT) or Modulation Doped field Effect Transistor (MODFET) is the fastest transistor currently available and a suitable candidate for microwave and millimeter wave applications [1-2]. It is a hetero-structure device and the unique properties of HEMT are the presence of a two dimensional electron gas (2-DEG) at its interface [3]. Because of its high power handling capabilities, GaN based pHEMTs have attracted increasing interests [4-5]. Owing to its large band-gap, GaN is particularly suitable for high frequency, high power and high temperature applications [6-7]. In addition, AlGaN/GaN material is suitable for applications in the transmission and distribution of electric power [8-9]. The AlGaN/GaN pHEMT is an attractive option for various radar, communication and satellite applications in the high frequency range [10-11]. AlGaN/GaN pHEMTs have breakdown voltages in excess of 100V, which eliminates the need for protection circuitry, such as in a front-end receiver, making an AlGaN/GaN based design less complex with lower noise [12]. AlGaN/GaN has also lower electron mobility and high electron velocity making it useful at high frequencies. Since, these values of electron mobility and electron velocity translate into a good unity current gain (f_T) and maximum frequency of oscillation (f_{max}), so, it also performs well for noise [13]. The short channel effects and parasitic resistances deteriorate the microwave performance of the device. So, it is significant to figure out the extrinsic and intrinsic factors behind the electrical degradation of

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AlGaN/GaN pHEMTs. In the present work, these factors have been improved to use this device over a wide range of operation. [14-15].

In the present work, a non-linear DC model for AlGaN/GaN MODFET is developed, based on the AlGaAs/GaAs system proposed by N. Dasgupta *et al.* [16] which is used to formulate the I-V characteristics from sub-threshold to high conduction region. The effects of source and drain resistances have also been included in order to find the extrinsic characteristics. Both intrinsic and extrinsic small-signal parameters such as transconductance, drain/output conductance and cut-off frequencies have also been evaluated. The present model is valid in the linear region and can be extended in the saturation region also.

2. Model Formulation

In this section, an analytical model of a AlGaN/GaN MODFET is presented. The basic structure of the AlGaN/GaN MODFET for the present work is shown in Figure1.

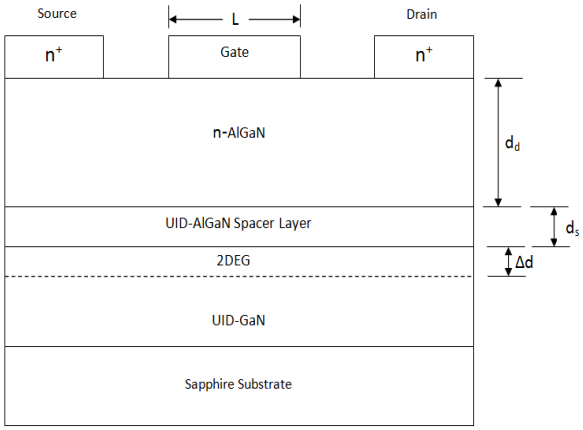

Figure 1. Cross-sectional view of 2-DEG MODFET

The threshold voltage V_{th} of the doped structure can be expressed as:

$$V_{th} = \Phi_m - \Delta E_c - \frac{qN_d d_d^2}{2.\varepsilon}(1+\frac{2.d_s}{d_d}) \quad (1)$$

where Φ_m is the Schottky barrier height, ΔE_c is the conduction band discontinuity at heterojunction, N_d doping density of the AlGaN layer, $d = d_d + d_s + \Delta_d$ is the separation between the gate and the channel, d_d is the doped AlGaN layer thickness, d_s is the undoped AlGaN spacer layer thickness, Δ_d is the effective width of the 2DEG. In the foregoing section, an attempt is made to obtain the various parameters of the proposed model such as transconductance, drain conductance etc. analytically by taking the parasitic resistances into account.

2.1. Intrinsic Characteristics

The drain current in the channel for AlGaN/GaN MODFET can be written [17] as:

$$I_d = qZn_s(x)v(x) \quad (2)$$

Where q is the electron charge, Z is the gate width and $v(x)$ is the electron charge carrier velocity, $n_s(x)$ is the 2-DEG sheet charge carrier concentration in an AlGaN/GaN MODFET and is given as:

$$n_s(x) = \frac{\varepsilon(m)}{qd}\{V_{gs} - V_{th} - V_c(x)\} \tag{3}$$

Where $\varepsilon(m)$ is the dielectric constant, m is the Al mole fraction, V_{gs} is the gate-source voltage, $V_c(x)$ is channel potential at any point x due to drain voltage.

For simplicity, the following velocity-field relation is assumed to be valid for carrier transport in the channel:

$$\begin{aligned} v(x) &= \frac{\mu_0 \dfrac{dv(x)}{dx}}{1+\dfrac{1}{E_c}\dfrac{dv(x)}{dx}} \quad for E_x < E_c \\ &= V_{sat} \qquad for E_x > E_c \end{aligned} \tag{4}$$

Where $E_x = \dfrac{dv(x)}{dx}$ is the electric field at any point x in the channel, $V_c(x)$ is the channel potential at point x due to drain voltage, μ_o is the low field mobility, and E_c is the critical field given by $E_c = V_{sat}/\ \mu_o$ and V_{sat} is the saturation velocity of the electrons. .

2.1.1. Linear Region

The electron velocity is less than the saturation velocity V_{sat} for lower drain voltages. By substituting eq. (2) in eq.(1) $for E_x < E_c$ and using eq.(3), the drain current in the linear region can be obtained as:

$$I_{ds} = \frac{qZ\mu_0 \dfrac{dv(x)}{dx}}{1+\dfrac{1}{E_c}\dfrac{dv(x)}{dx}}\left[\frac{\varepsilon(m)}{qd}\{V_{gs} - V_{th} - V_c(x)\}\right] \tag{5}$$

After solving eq. (5) using boundary conditions $V(x) = 0$ for $x = 0$ and $V(x) = L$ for $x = L$, the current flowing through the 2DEG is found to be:

$$I_{ds} = \frac{\varepsilon Z\mu_0}{d\left(L + \dfrac{V_{ds}}{E_c}\right)}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{6}$$

Where L is the gate length of the device.

2.1.2. Saturation Region: The channel voltage increases from source to drain, the electric field is maximum close to the drain, and the velocity saturation occurs first at the drain side of

the gate region. At the drain end of the channel, the velocity of the electrons saturates to V_{sat}. Thus from eq. (4) *for* $E_x > E_c$, the drain current can be given as:

$$I_{dsat} = qZn_s(x)v_{sat} \tag{7}$$

Using eq. (4) and eq. (7), with $V_c(x) = V_{dsat}$, I_{dsat} is given as:

$$I_{dsat} = \frac{Z\varepsilon v_{sat}}{d}\left(V_{gs} - V_{th} - V_{dsat}\right) \tag{8}$$

The saturation drain voltage can be calculated analytically by equating eq. (8) and eq. (6) with $V_d = V_{dsat}$ as:

$$A_1V_{dsat}^2 + A_2V_{dsat}^2 + A_3 = 0 \text{ or}$$

$$V_{dsat} = \frac{-A_2 + \sqrt{A_2^2 - 4A_1A_3}}{2A_1} \tag{9}$$

Where

$$A_1 = \frac{\mu E_c - 2v_{sat}}{2E_c},\ A_2 = (V_{gs} - V_{th})\left(\frac{V_{sat} - \mu E_c}{E_c}\right) - LV_{sat} \text{ and } A_3 = (V_{gs} - V_{th})Lv_{sat}$$

2.1.3. Transconductance: It is a measure of device gain and cut-off frequency. Mathematically, it is given as:

$$\mathrm{g_m} = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}} \tag{10}$$

Transconductance in linear region can be obtained by differentiating eq. (6) w.r.t. V_{gs}.

$$g_m = \frac{Z\mu\varepsilon V_{ds}}{d\left(L + \frac{V_{ds}}{E_c}\right)} \tag{11}$$

2.1.4. Drain Conductance: It is also a measure of the device gain. Mathematically, it is given as:

$$\mathrm{g_d} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}} \tag{12}$$

Drain conductance in linear region can be obtained by differentiating eq. (6) w.r.t. V_d

$$g_d = \frac{Z\mu_0\varepsilon}{d\left(L + \frac{V_{ds}}{E_c}\right)}(V_{gs} - V_{th} - V_{ds}) + \left\{(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right\}\left\{-\frac{1}{E_c}\left(\frac{Z\mu_0\varepsilon}{d(L + \frac{V_{ds}}{E_c})^2}\right)\right\} \tag{13}$$

2.2. Extrinsic Characteristics

As the gate length approaches the submicron region, parasitic resistances become comparable with channel resistances and can't be neglected. Incorporating the parasitic resistances R_s and R_d into account, the gate and drain voltages are thus modified as follows:

$$\begin{aligned} V_{ds} &\to V_{ds} - I_{ds}(R_s + R_d) \\ V_{gs} &\to V_{gs} - I_{ds}R_s \end{aligned} \tag{14}$$

2.2.1. Linear region: Considering the above conditions, the drain current in the linear region can be obtained from eq. (8) as:

$$B_1 I_{ds}^2 + B_2 I_{ds} + B_3 = 0$$

$$I_{ds} = \frac{-B_2 + \sqrt{B_2^2 - 4B_1 B_3}}{2B_1} \tag{15}$$

Where

$$B_1 = (R_s + R_d)\left\{\frac{d}{E_c} + \frac{\varepsilon\mu Z}{2}(R_s - R_d)\right\} \quad ,$$

$$B_2 = -dL - \frac{d}{E_c}V_{ds} - \varepsilon\mu Z(R_s + R_d)\left[V_{gs} - V_{th} - V_d\right] - \varepsilon\mu Z R_s V_d$$

And $B_3 = \varepsilon\mu Z(V_{gs}V_{ds} - V_{th}V_{ds} - \frac{V_{ds}^2}{2})$

2.2.2. Saturation region: The drain current in saturation region can be obtained analytically from eq. (8) with $V_d = V_{dsat}$,

$$I_{dsat} = \frac{Z\varepsilon v_{sat}}{d}\left(V_{gs} - V_{th} - V_{dsat} + I_{dsat}R_d\right) \tag{16}$$

The extrinsic saturation drain voltage can be obtained numerically by equating eq. (15) at $V_d = V_{dsat}$ with eq. (16)

$$V_{dsat} = \frac{-\delta_2 + \sqrt{\delta_2^2 - 4\delta_1\delta_3}}{2\delta_1} \tag{17}$$

Where

$$\delta_1 = \frac{Q}{P}\left(A\frac{Q}{P} + \frac{d}{E_C}\right) - \frac{\varepsilon\mu Z}{2}\left(2\frac{Q}{P}R_d + 1\right)$$

$$\delta_2 = \left(V_{gs} - V_{th}\right)\left[\frac{Q}{P}\left(R_d\varepsilon\mu Z - \frac{d}{E_C}\right) + \varepsilon\mu Z\right] - \frac{Q}{P}\left[2\left(V_{gs} - V_{th}\right)A\frac{Q}{P} - dL - R_{ss}\varepsilon\mu Z V_{gs} + R_{ss}\varepsilon\mu Z V_{th}\right]$$

$$\delta_3 = \frac{Q}{P}\left(V_{gs} - V_{th}\right)\left(A\frac{Q}{P}\varepsilon\mu Z - dL - R_{ss}\varepsilon\mu Z V_{gs} + R_{ss}\varepsilon\mu Z V_{th}\right)$$

And

$Q = \frac{Z\varepsilon V_{sat}}{d}$, $P = 1 - R_d Q$ and $R_{ss} = R_s + R_d$

2.2.3. Transconductance: Transconductance in the linear region can be obtained by differentiating eq. (15) w.r.t. V_g

$$g_m = \frac{1}{2B_1}\left[-\varepsilon\mu Z(R_s + R_d) + \frac{1}{2\sqrt{B_2^2 - 4B_1B_2}} \left\{ 2B_2(-\varepsilon\mu Z(R_s + R_d)) - 4B_1\varepsilon\mu Z V_{ds} \right\} \right] \quad (18)$$

2.2.4. Drain conductance: The drain conductance can be obtained numerically by differentiating eq. (15) w.r.t. V_d

$$g_d = \frac{1}{2B_1}\left[\{ -\frac{d}{E_c} - \varepsilon\mu Z(2R_s + R_d) + \frac{1}{2\sqrt{B_2^2 - 4B_1B_3}} \left\{ 2B_2\{ -\frac{d}{E_c} - \varepsilon\mu Z(2R_s + R_d) - 4B_1(\varepsilon\mu Z(V_{gs} - V_{th} - V_{ds}) \right\} \right] \quad (19)$$

3. Capacitance-Voltage Characteristics

Total channel charge is given [17] as:

$$Q = \int_0^t I_{ds} dt = \int_0^L \frac{I_{ds}}{v(x)} dx \quad (20)$$

Rearranging (2) and using (3), we get

$$\frac{Ids}{v(x)} = \frac{Z\varepsilon(m)}{d}\left(V_{gs} - V_{th} - V_c(x)\right) \quad (21)$$

Integrating eq. (21)

$$\int_0^L \frac{I_{ds}}{v(x)} dx = \frac{Z\varepsilon(m)}{d} \int_0^L \left(V_{gs} - V_{th} - V_c(x)\right) dx \quad (22)$$

Using [18]

$$dx = \frac{Zqn_s(x)\mu - \frac{I_{ds}}{E_1}}{I_{ds}} dV_c(x) \quad (23)$$

Substituting eq. (23) into eq. (22), total charge is given as:

$$Q = \frac{z\varepsilon(m)}{d} \int_0^L \left(V_{gs} - V_{th} - V_c(x)\right) \left\{ \frac{Zqn_s(x)\mu_0 - \frac{I_{ds}}{E_3}}{I_{ds}} \right\} dV_c(x) \quad (24)$$

On solving eq. (24),

$$Q = \frac{-z^2\varepsilon^2(m)\mu_0}{3d^2 I_{ds}}\left[\left(V_{gs}-V_{th}-V_{ds}\right)^3-(V_{gs}-V_{th})^3\right]-\frac{Z\varepsilon(m)}{dE_3}V_{ds} \quad (25)$$

3.1. Gate-Drain Capacitance

It is also called as feedback capacitance. It is defined as the rate of change of charge on the gate electrode with respect to the drain bias when the source and the gate potentials are kept constant.

$$C_{ds} = \frac{\partial Q}{\partial V_{gs}} = \frac{R}{I_{ds}}(V_{gs}-V_{th}-V_{ds})^3 - \frac{Z\varepsilon(m)}{dE_3} \quad (26)$$

3.2. Gate-Source Capacitance

The gate-source capacitance (C_{gs}) is defined as the change in total charge with the change in gate voltage. It is mainly due to the 2DEG in the normal operating region, and is given as

$$C_{gs} = \frac{\partial Q}{\partial V_{gs}} = \frac{R}{I_{ds}}\left[(V_{gs}-V_{th})^2-(V_{gs}-V_{th}-V_{ds})^2\right] \quad (27)$$

4. Cut-off Frequency

It is one of the primary figure of merit for microwave performance, which can be obtained as;

$$f_c = \frac{g_m}{2\pi C_g} \quad (28)$$

Where

$C_g = \frac{\varepsilon(m)LZ}{d}$ = effective gate capacitance for linear region.

LZ is the effective area under the gate.

Finally, the parameters of the proposed model are obtained analytically in the above sections.

5. Results and Discussion

The characteristics of AlGaN/GaN MODFET have been modeled and the results obtained are compared with the previous simulated results to prove the validity of the model. The intrinsic and extrinsic characteristics are also plotted to predict the effect of parasitic resistances.

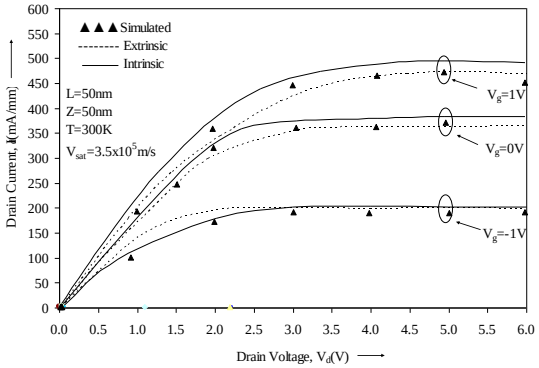

Figure 2. Dependence of Drain Current on Drain Voltage for different values of gate voltage

The variation of drain current with drain voltage for intrinsic and extrinsic cases at different gate voltages is depicted in Figure 2. A small variation in extrinsic and intrinsic characteristics is observed for smaller gate voltages. The difference between intrinsic and extrinsic characteristics shows that the analysis without parasitic source and drain resistances, *i.e.*, intrinsic case results in low saturation voltage and higher drain currents. Taking into account these parasitic resistances, *i.e.*, extrinsic case, close agreement with the simulated results are obtained. This is because increase in channel resistance as gate voltage decrease. Due to increase in channel resistance, the effect of parasitic resistance becomes negligible. A high saturation current of 502.6mA/mm at a gate bias of 1V is achieved. The calculated results are in good agreement with the simulated results [19].

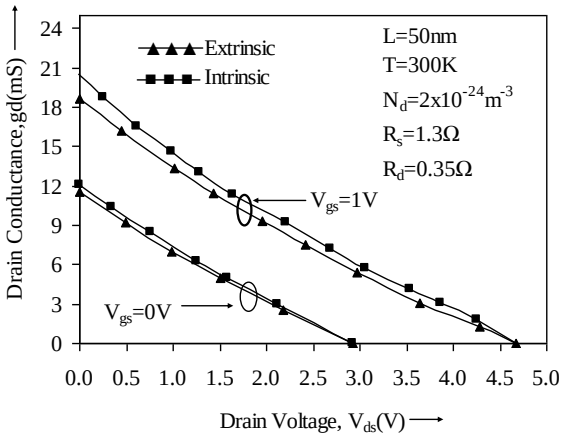

Figure 3. Variation of drain conductance with drain voltage for various gate bias

Figure 3 shows the dependence of output conductance on drain voltage for different gate biases. As depicted in the figure, with the increases in drain voltage, the drain/output conductance decreases sharply and finally becomes zero. The g_d decreases with increases in V_g, the channel resistance decreases and the g_d increases with increase in gate voltage.

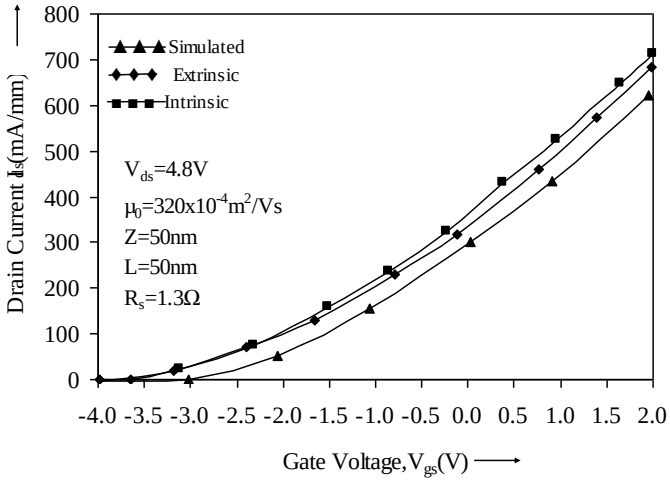

Figure 4. Dependence of drain current on gate voltages

The variation of drain current with gate voltage is depicted in Figure 4. Figure shows that with increase in gate voltage, the drain current also increases. The extrinsic characteristics are found to be closer to the simulated results. The discrepancy observed at higher gate voltages. The analytical results are in close proximity with the previous published results [19].

The variation of transconductance with gate voltage is shown in Figure 5. The transconductance increases with gate voltage in the linear region. The transconductance decreases with the increase in negative gate bias as the depletion layer width increases and channel width decreases. The transconductance of 33.2 mS and 32.3 mS respectively are observed for intrinsic and extrinsic cases.

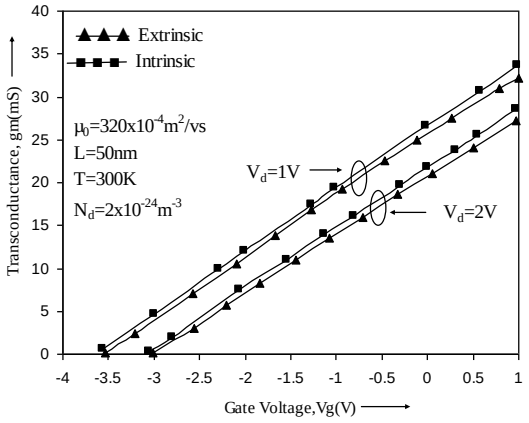

Figure 5. Dependence of Transconductance on Gate Voltage

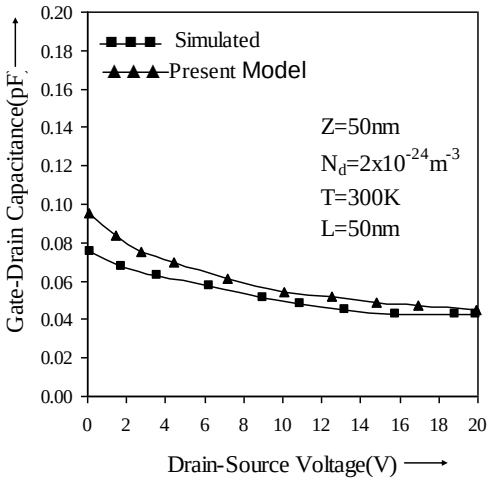

Figure 6. Dependence of gate-drain capacitance on drain source voltage

The variation of gate-drain capacitance with drain bias is depicted in Figure 6. It can be observed from the figure that the capacitance decreases gradually with increase in drain voltage. The calculated results are in good agreement with the previously simulated results [20].

The dependence of gate-source capacitance on gate voltage is shown in Figure 7. It is evident from the Figure 7 that C_{gs} decreases with increase in negative gate bias because of the increase in depletion layer width. The analytical results are in good agreement with the previously published results [20].

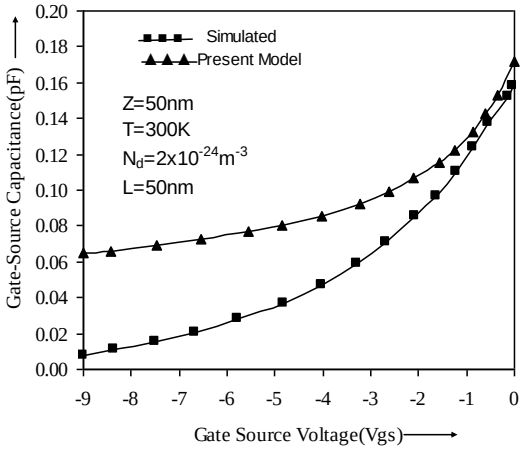

Figure 7. Variation of gate-source capacitance with gate-source voltage

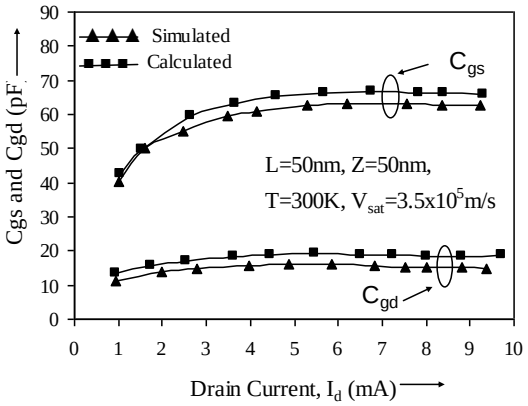

Figure 8. Dependence of gate to source capacitance and gate to drain capacitance on drain current

The variation of gate-source capacitance and gate-drain capacitance with drain current is shown in Figure 8. It can be seen from the figure that the gate-source capacitance increases with increase in the saturation current because of the increase in gate-source voltage. Also gate-source capacitance is almost constant in the saturation region. The calculated results are in close agreement with the previously published results [21].

The dependence of cutoff frequency with gate voltage for both extrinsic and intrinsic cases is plotted in Figure 9. The cutoff frequency increases with gate voltage and then saturates. The highest cutoff frequencies for both intrinsic and extrinsic cases are observed at 22.5GHz and 21.3 GHz, respectively.

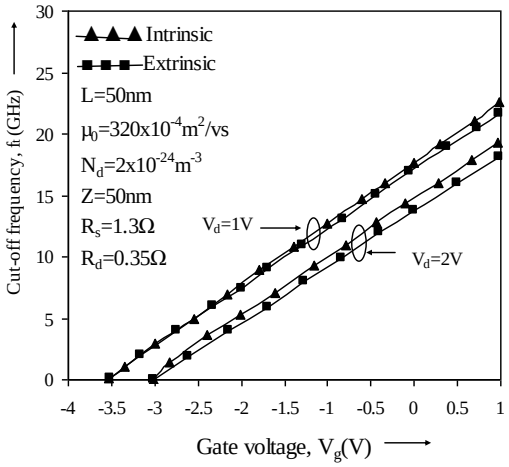

Figure 9. Variation of cut-off frequency with gate voltage

In nutshell, it is observed from the above figures that the results are in close agreement with the previously published results and hence prove the validity of the model.

6. Conclusion

A compact and accurate analytical model is developed for the I-V characteristics and small-signal parameters of an AlGaN/GaN MODFET. The model presented in this paper includes the effects of parasitic resistances R_s and R_d into account. The model showed a high saturation current of 502.6mA/mm at a gate bias of 1V. A high cut-off frequency of 22.5 GHz is obtained at a drain bias of 1 V for a 50nm gate length. The expression obtained are fully analytical and do not have any fitting parameters. The need for incorporating the effect of parasitic resistance at higher gate, lower drain voltages and submicron gate length of the device is emphasized. The obtained results are in close agreement with the previously published results proving the validity of the model. The results indicate that the AlGaN/GaN MODFET is suitable for microwave and millimeter wave circuit applications.

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