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Influence of High-k Gate Dielectric on Nanoscale DG-MOSFET

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Abstract

Influence of dielectric materials as gate oxide on various short channel device parameters using a 2-D device simulator has been studied in this paper. It is found that the use of high-k dielectrics directly on the silicon wafer would degrade the performance. This degradation is mainly due to the fringing field effect developed from gate to source/drain. This fringing field will further generate electric field into the channel region from source/drain region which weakens the gate control. Therefore, by taking the gate stack engineering into account it has been shown that the induced electric field along the channel can be minimized as well as the device performance can be enhanced. This paper examined various parameters of the device like potential distribution from source and drain, threshold voltage (V_{th}), drain induced barrier lowering (DIBL), subthreshold slope (SS), on-current (I_{on}), off-current (I_{off}) and Transconductance (g_m) by taking different dielectric materials [SiO_2(ε=3.9), Si_3N_4 (ε=7.5), HfO_2 (ε=24) and Ta_2O_5 (ε=50)] as gate oxide (s).

Keywords: *Double gate MOSFET, High-k dielectric, Gate stack, Short channel effects (SCES), Equivalent oxide thickness (EOT)*

1. Introduction

The major limitation in scaling of CMOS devices is the gate dielectric thickness [1-3]. The conventional SiO_2 as gate dielectric has reached the point where film thickness is only a few atomic layers thick. At these dimensions or below 1.5 nm, the direct tunnelling dramatically increases the leakage current which, consequently increases the static power and hence affect the circuit operation as suggested by CAMPBELL *et al.* & RIBES *et al.* [4-5]. To get rid of this critical problem, high-k dielectrics have been introduced by taking directly on the silicon wafer or on the SiO_2 layer. While keeping the equivalent oxide thickness (EOT) constant, high-k dielectrics permits the increase in physical thickness (a factor of k/k_{SiO2}) of the gate oxide to inhibit gate tunnelling [5-6]. However, it has been verified by device simulation that the use of high-k gate dielectrics directly on silicon wafer would degrade the short channel performance. This degradation is mainly caused by the fringing fields either from the gate to the source/drain regions or from the source/drain to the channel region which weakens the gate control [7]. But these shortcomings to some extent can be overcome by taking the gate stack (GS) configuration, *i.e.*, high-k dielectrics over SiO_2 layer [8-11]. By taking a thick layer of dielectric material over a thin SiO_2 layer keeping EOT constant significantly reduces the gate tunnelling current.

In addition, there are various limitations with the use of high-k gate dielectrics : 1) the use of high-k dielectrics results in poly silicon gate depletion effects and finite inversion layer

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(FIL) capacitance [6]. Gate depletion in current poly silicon gate technology increases the effective gate thickness and degrades the device performance. Therefore, to mitigate this problem, it is desirable to replace the poly silicon gate with mid-gap gates or metal gates. 2) Another challenge for integrating high-k is the threshold voltage stability during operation. The shift in V_{th} known as hysteresis phenomenon is attributed to trapping of charges in the pre-existing traps without creation of additional traps. This problem is somewhat mitigated by considering the Hafnium (Hf)-based dielectrics [4].In this work, extensive simulations have been carried out to study the performance degradation due to fringing fields in high-k dielectrics and its minimization by considering gate stack engineering. Different GS configurations are simulated to optimize the device performance by integrating high-k dielectrics into various structures..

2. Device Design and Structure

The schematic structure of DG MOSFET is shown in Fig. 1. In this structure both the channel length (L) and Source/Drain length (L_S/L_D) are fixed as 40nm, the silicon thickness (t_{Si}) is taken as 10nm and a uniform density of N_D is taken as 10^{20} cm^{-3} . The channel is doped (N_A) with 10^{16} cm^{-3}. Two different types of structural models have been considered. The first model is structured considering single oxide layer and the second with double oxide layer or gate stack . In each case the EOT is fixed at 1.1nm. To maintain a constant capacitance for k=7.5, k=24 and k=50, the corresponding high-k thicknesses are 2.1nm, 6.8nm and 14.1nm respectively for single layer configurations. Further for double layer/GS configurations SiO_2 layer thickness is fixed at 0.6nm and above this layer 0.5nm equivalent thickness of high-k layer is deposited, so that the EOT reaches 1.1nm. This work considers the high-k dielectrics as Si_3N_4, HfO_2 and Ta_2O_5 and the work function for the gate material is taken as 4.8eV.

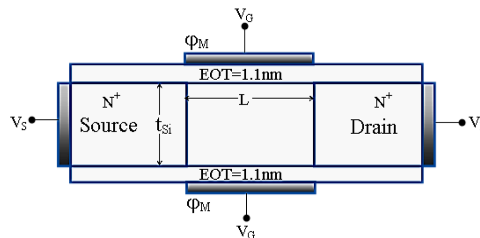

Figure 1. Schematic structure of Double Gate N-MOSFET

3. Device Simulation

To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The degradation is normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. So in the simulation the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model was considered. The Shockley–Read–Hall (SRH) model simulates the leakage currents that exist due to thermal generation. Electrons in thermal equilibrium at given temperature with a semiconductor lattice obey Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory, however, Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact values. Auger recombination models for minority carrier recombination have been used.

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Furthermore, we chose Gummel's method (or the decoupled method) which performs a Gummel iteration for Newton solution [12].

4. Results and Discussion

In Figure 2 & 3, I_D-V_{GS} transfer characteristics have been shown on linear scale and log scale for different device structures. Here different dielectric materials are considered as gate oxide for both single and double layer configurations and their characteristics have been analyzed for V_{DS}=0.1V and 1.2V. The Sub threshold Slope (SS) is the major parameter for calculating the off state current. Furthermore, SS is calculated as:

$$SS(mV/dec) = \frac{\partial V_G}{\partial(\log I_D)} \qquad (1)$$

The typical value for the SS of Multigate MOSFET is 60 mV/decade. In this paper the SS is extracted by calculating the inverse of maximum slope of V_{GS} versus log (I_D) curve as shown in the TABLE 1. Therefore, comparing the values in TABLE 1, it is clear that with increasing high-k dielectric permittivity for the single oxide layer configurations , the SS value increases and reaches a value 75.53 mV/decade. But, for double layer/gate stack configuration the SS value nearly approaches the ideal value.

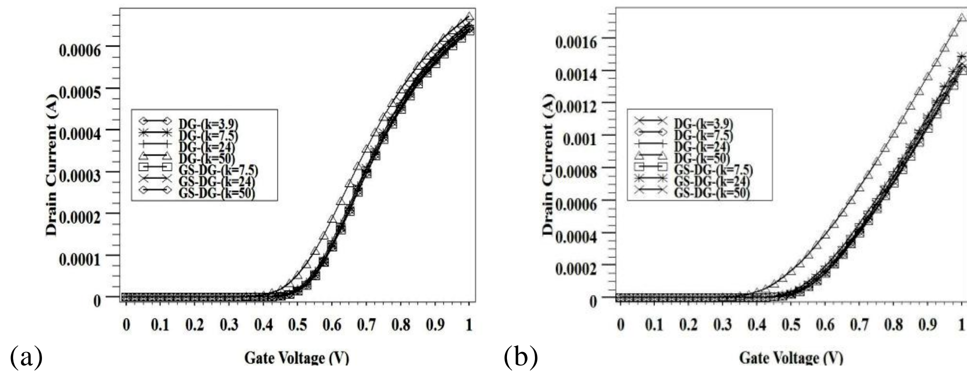

Figure 2. Behaviour of Drain Current (I_D) as a function of Gate Voltage (V_{GS}) in linear scale at (a) V_{DS}=0.1V (b) V_{DS}=1.0V

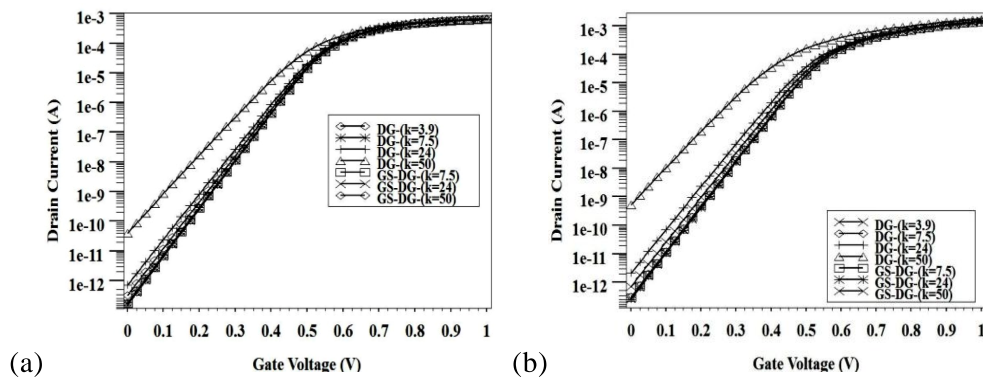

Figure 3. Behaviour of Drain Current (I_D) as a function of Gate Voltage (V_{GS}) in log scale at (a) V_{DS}=0.1V (b) V_{DS}=1.0V

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The V_{th} is also a very important parameter for higher on state current. The V_{th} is amount of V_{GS} when the I_D is equal to $1x10^{-6}$A. The extraction is given in Table 1. It is observed that for single oxide layer configuration at k=50 shows higher I_{on}. But, at the same time it also offers a undesirable higher leakage current (I_{off}) in the order of 59pA. The g_m versus V_{GS} characteristics have been compared for different device structures as shown in Fig.4. As we know:

$$g_m = \partial I_D / \partial V_{GS} \qquad (2)$$

The value of g_m is extracted by taking the derivative of I_D-V_{GS} curve & the values are summarized in Table 2. It is observed from the said table that the GS configurations are showing higher values of g_m.

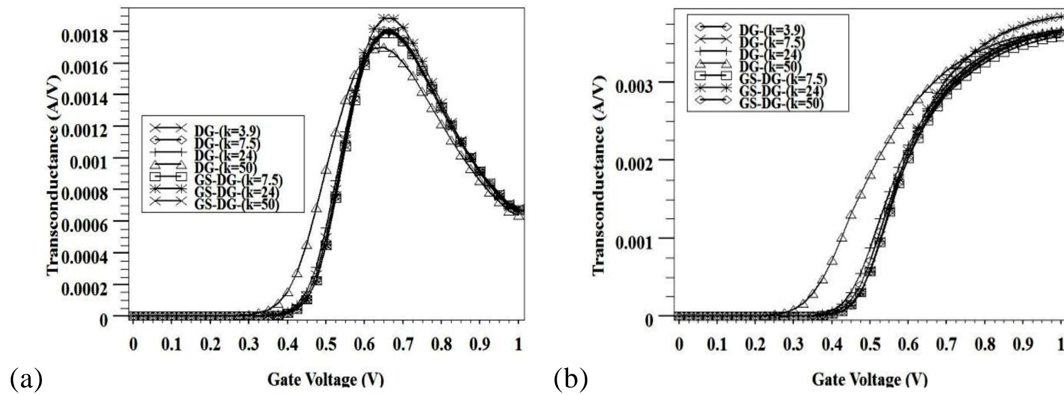

Figure 4. Variation of transconductance (g_m) with V_{GS} for different configurations at (a) V_{DS}=0.1V (b) V_{DS}=1.0V

The value of DIBL is calculated as per the relation :

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} \qquad (3)$$

The GS structures shows better values of DIBL as compared to single layer structures.

Table 1. Extracted Device Parameters for Different Cofigurations

Configuration	SS (mV/dec)	I_{on}(mA/μm)	V_{th}	SS (mV/dec)	I_{on}(mA/um)	V_{th}
	At V_{DS}=0.1V			At V_{DS}=1V		
DG k=3.9	62.01	0.64	0.422	62.22	1.41	0.409
DG k=7.5	62.15	0.64	0.421	62.32	1.42	0.407
DG k=24	65.13	0.65	0.403	65.37	1.48	0.377
DG k=50	75.53	0.67	0.337	76.34	1.73	0.255
GS-DG k=7.5	62.06	0.64	0.422	62.25	1.40	0.408
GS-DG k=24	61.80	0.66	0.423	61.94	1.49	0.410
GS-DG k=50	63.42	0.64	0.412	63.67	1.44	0.395

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The I_{off} is extracted by calculating the I_D at $V_{GS}=0$ and $V_{DS}=V_{DD}$. It is important to keep I_{off} very small in order to minimize the device static power dissipation. From TABLE 2, it is clear that the I_{off} value is very low for GS configuration which is one of the desired performance of the Device.

Table 2. Extracted Parameters

Configuration	I_{off} (pA) at V_{DS}=0.2V	g_m (mS) at V_{DS}=0.1V	g_m (mS) at V_{DS}=1V	DIBL (mV/V)
DG (k=3.9)	0.393	1.81	3.63	14.863
DG (k=7.5)	0.397	1.82	3.64	15.019
DG (k=24)	0.845	1.81	3.66	29.342
DG (k=50)	59.028	1.71	3.65	90.308
GS-DG k=7.5)	0.394	1.80	3.58	14.937
GS-DG (k=24)	0.390	1.90	3.84	14.254
GS-DG (k=50)	0.430	1.81	3.63	19.269

Figure 5 represents the variations of DIBL, V_{th} and SS values as a function of dielectric permittivity (k) for both single layer and double layer configurations

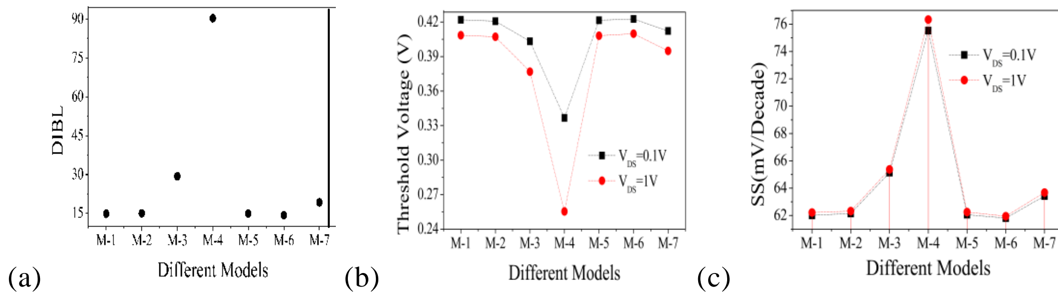
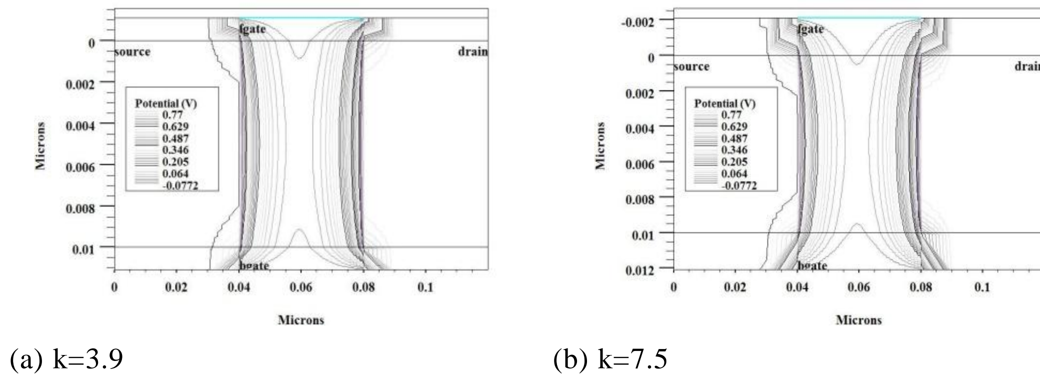


Figure 5. Variation of DIBL (a), Threshold Voltage (b) and SS (c) as a function of gate dielectric permittivity (k) for different configurations



(a) k=3.9 (b) k=7.5

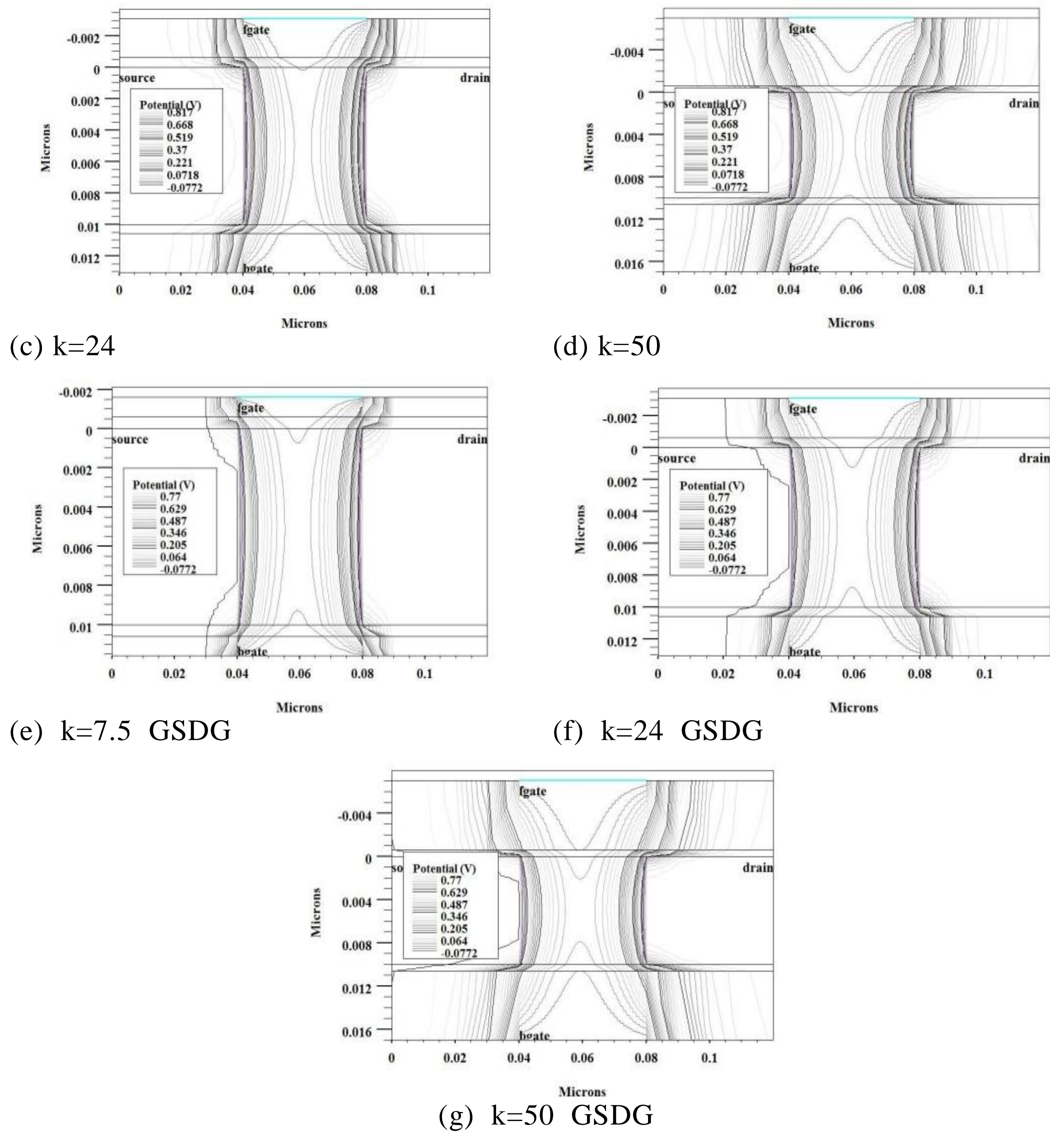


Figure 6. The simulated results of the potential distribution in the gate insulator for different configurations keeping EOT as 1.1nm in each case. Figure for single layer configuration with k=3.9 (a), for single layer configuration with k=7.5 (b), for single layer configuration with k=24 (c), for single layer configuration with k=50 (d), for double layer/GS with k=7.5 (e), for double layer/GS with k=24 (f) and for double layer/GS with k=50 (g)

Figure 6 shows the potential distribution of different device structures by considering various gate dielectric materials to investigate the effect of the fringing fields from source and drain through the gate insulator. By comparing the single layer structures shown in Figure 6 (b), (c) and (d), it is observed that with increasing k value (i.e. for k=7.5, 24 and 50), the electric fields from the source to the drain spread into the channel area. This results in lowering of the channel barrier potential and induces the short channel effects. However, from the structures shown in Figure 6 (e), (f) and (g)

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with double layer/GS, the electric field lines gradually decreases from the channel. As a result the electrostatic interiority of the device is maintained.

5. Conclusion

The impact of high-k gate dielectrics on short channel effects in both single and double layer gate oxide structures have been studied. The degradation in short channel performance of the device is analyzed by using ATLAS 2D device simulator. This paper investigates the effect of fringing fields from the source and drain to the channel region for different structures with varying dielectric permittivity. It is found that the degradation in short channel performance using high-k dielectrics is mainly due to the fringing fields from the gate to the source/drain regions. This work also shows that better short channel performance can be achievable by taking GS/double layer configurations for the DGMOSFET. It is possible to suppress the fringing fields, I_{off}, SS and DIBLvalues & also to improve the performances of the nano scale DGMOSFET by considering a gate stack architecture using a thick layer of high-k dielectric material above a thin layer of SiO_2 maintaining constant EOT.

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