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Analyze the Tunneling Effect on Gate-All-Around Field Effect Transistor

Awanit Sharma[1] and Shyam Akashe[2]

[1]*Reasearch Scholar of ITM Universe, Gwalior, India*
[2]*Associate Professor, Department of Electronics Instrumentation*
ITM University, Gwalior, India

awanitsharma@gmail.com, shyam.akashe@yahoo.ac.in

Abstract

In this paper we describe the tunneling junction model effect on silicon nanowire gate-all-around field effect transistor using CMOS 45 nm technology. Tunneling effects provides better subthreshold slope, excellent drain induced barrier lowering and superior ION-IOFF ratio.This paper demonstrates the gate controlled tunneling at source of Gate-all-around field effect transistor. Low leakage current (off current) is reported of 2.9uA with considerable power reduction Subthreshold Swing SS is achieved of 46.5 mV/dec .Using Y function series resistance RSD is evaluated.Accurate evaluation of RSD of silicon nanowire Gate-all-around FET is shown linear behavior in inversion region using Y function. Silicon nanowire is considered as better aspect for ultra low power application.

Keywords: *Tunneling junction model; Silicon nanowire; Gate-all-around (GAA); Y function; Drain induced lower barrier (DIBL); Subthreshold Slope*

1. Introduction

The tunneling field-effect transistor (TFET) has a better prospect that it could be considered as promising application for ultra low power [1-10]. The reduction of leakage current I_{OFF} and necessary factor that subthreshold slope (SS) is not confined to kt/q.Tunneling junction model provide the same functionality as TFET. Silicon nanowire Gate-All-Around (GAA) Field effect transistor has researched excellent electrostatic control over the channel surrounded by conducting gate and higher transconductance [11]. Simulation and analysis show's gate-all-around GAA configuration provide the excellent performance owing to considerable effect of short channel as compared with other structures. The performance of relative transistors is drastically reduced as the scaling of channel length occur.There is to need of transistors having SS below 50 mV/decade for ultra low power application [1, 12]. In tunneling junction model transportation of carrier is defined by tunneling across barrier but in conventional FET diffusion over barrier occurs.We here simulate the new tunneling junction model similar to TFET in which tunneling is in normal direction to the gate. Gate-all-around (GAA) nanowire (NW) transistor's concept are promising one due to better gate coupling, top-down approach for functionality of circuit [13]. On-current Whenever scaling of channel length is to be done I_{ON} current is not affected due to tunneling voltage counterpart. I_{ON} is independent and does not affect by channel

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length, but scaling of channel length be however relaxed.On current is dependent on size of the transistor where size dependence can be described as

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 \quad (1)$$

$$\beta = \frac{\mu\epsilon}{Tox} \times \left(\frac{W}{L}\right) \quad (2)$$

Active power dissipation that is calculated by

$$\mathrm{P} = \mathrm{C}V^2\mathrm{f} \quad (3)$$

Where C is considering as capacitive load, V is defined as applied voltage, and f is the frequency. Active power dissipation can be defined for gains result as reduction of applied voltage. Here we define a tunneling junction model similar effects as TFET provides the increment of tunneling cross section to offer the high on-current I_{ON} and provide lower subthresold slope SS due to tunneling occurs uniformly through junction of transistors [14]. In Silicon nanowire FET, the series resistance R_{SD} is to be considered as parameter that is important and directly dependent on scaling of channel length [15, 16]. Channel scaling is offers channel resistance due to electron mobility enhancement. As channel scale down R_{CH} become smaller that degrade the performance .Scaling of channel offers the channel resistance R_{CH} that reduces to smaller value therefore it is important to keep series resistance R_{SD} smaller than R_{CH}. However, a fraction of the applied voltage dropped across R_{SD} is observed therefore variation and degradation of current occur.

2. Design and Analysis of Tunneling Junction Model

In Gate-all-around FET process, current is doubled or tripled due to tunneling effect that shows benefit of surrounding gate structure. ON-current is boosted and get higher, while the leakage (OFF current), still lower but increases by the same ratio and still low. When volume inversion takes place this effect could be higher. Gate leakage current decrease by high order of magnitude.Energy quantization effect is described on tunneling current at respective gate of gate-all-around silicon nanowire FET.

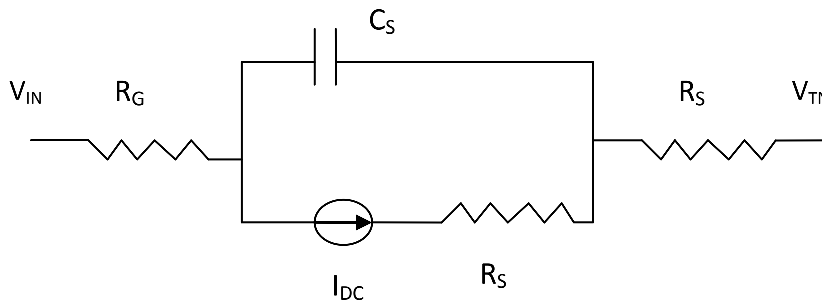

Figure 1. Schematic of tunneling junction model

This circuit is capable provide electron tunneling by keeping Idc to suitable value. Series resistance with dc current source and parallel capacitor provide higher mobility of carriers that enhancement carriers and provide volume inversion. RS at tunneling junction VT provide drop in tunneling voltage to keep effect in the limit and not burn the FET. Silicon nanowire

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FET is affected as same manner as other or simple FET is affected. This circuit provides tunneling effect based on WKB approximation and gate electron tunneling effect is same for GAA as TFET. GAA configuration provide higher ON drive current due to better electrostatic control behavior.

Gate length is scaled down to 45 nm therefore estimated gate oxide thickness could be approximate to be below 2 nm. Whenever gate oxide thickness becomes smaller to 2 nm then biasing of FET by applying voltage to gate electrode, band bending observed near oxide-semiconductor overlap interface that create quantum well. Therefore energy quantization occurs and barrier height becomes finite to 3.1 eV for electrons. Direct tunneling current occurs due to silicon inversion layer provide gate leakage current. Thin oxide of MOSFETs is expected the direct tunneling current that much contributes to the leakage current. In this paper a tunneling junction model is developed for gate tunneling by introduce the model between gate and the source/drain region.

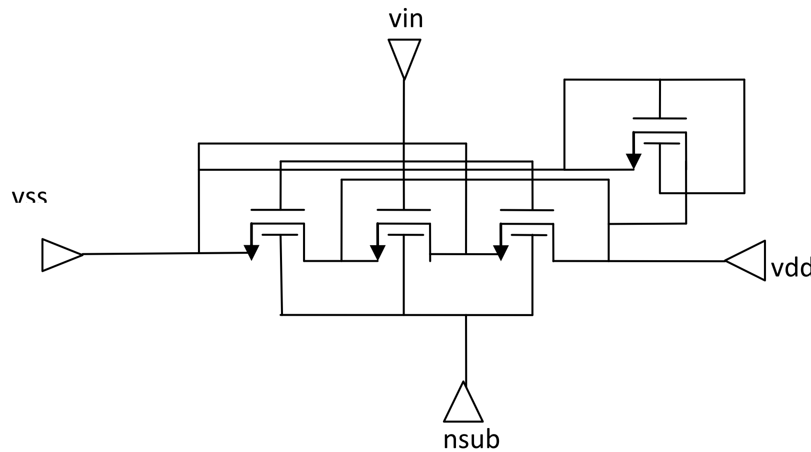

Figure 2. Schematic of silicon nanowire GAA n-FET

Tunneling concept lie on the quantum-mechanical effect that significantly describe the behavior of electrons that Electronic behavior can be described by wave function $\varphi(x, y, z)$ such that probability electrons in the region dxdydz are equivalent to $\varphi(x, y, z)^2 dxdydz$. Schrödinger electron wave function equation is shown as below

$$-\frac{\hbar^2}{2m}\nabla^2\varphi(x,y,z) + U(x,y,z)\varphi(x,y,z) = E\varphi(x,y,z) \tag{4}$$

Where $\hbar = h/2\pi$ is the Planck constant, m is the mass of electron, U is potential energy of electron and E is the energy of the charge carriers. Schrödinger equation solution is described the the quantitative analysis of tunneling. In channel region electron of energy E confine with barrier width is with of energy EV (eV) and width of channel in nm range. In the X direction that simply denote the region from source to drain through channel. Schrödinger equation can be described in channel region is defined as follows.

$$\frac{d^2\varphi}{dx^2} + k_1^2\varphi = 0 \qquad \text{for } x < 0 \tag{5}$$

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$$\frac{d^2\varphi}{dx^2} + k_2^2\varphi = 0 \qquad \text{for } 0 \le x \le d \tag{6}$$

$$\frac{d^2\varphi}{dx^2} + k_3^2\varphi = 0 \qquad \text{for } x \ge d \tag{7}$$

Where

$$k_1^{\,2} = k_3^{\,2} = \frac{2m}{\hbar^2} \tag{8}$$

$$K_2^{\,2} = n_b^2 k_1^2 \text{ and} \tag{9}$$

$$n_b^2 = \frac{(E - E_b)}{d} \tag{10}$$

Solution of the Schrödinger equation tunneling probability is given by expression

$$D(E) = e^{\frac{-2[2m(E_b - E)]^{1/2}d}{\hbar}} \tag{11}$$

This expression shows that greater value of barrier width and height is reduced the tunneling effect therefore MOSFETs with width of 45 nm likely to be higher tunneling effect and provide low leakage current. Tunneling voltage of 1.72 V at junction is evaluated with the help of cadence tool is shown in Figure 1.

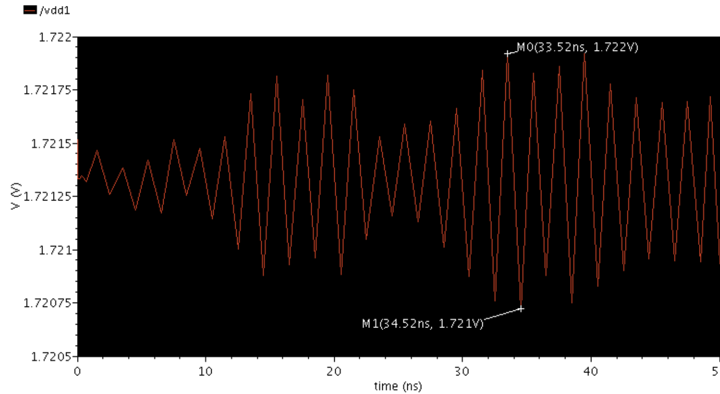

Figure 3. Shows V_{TN} Tunneling voltage at junction

Tunneling voltage provides electron tunneling at gate of FET. Threshold become lower due to gate tunneling that require enhancement of On drive current at lower gate to source voltage. Threshold is generally depended on saturated On drive current at weak inversion region that is shown by given equation.

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_T)^2 \tag{12}$$

Concept behind the tunneling effect is mainly due to electron therefore WKB approximation method is applicable to define the electron tunneling in Gate-all-around nanowire structure.

The WKB approximation is a method related to quantum electron tunneling effect that helpful to calculate the approximate solution of time-dependent one dimensional differential

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equation. It can be calculate the bound energy and tunneling rates through potential barriers.WKB approximation can be described by equation 12. Electron tunneling at gate is comprised of mainly three components but mainly depended on gate to source and gate to drain overlap current that dominate gate leakage in off state since gate to source and gate to drain overlap region become smaller than channel region therefore gate tunneling current minimum in off state minimize the leakage but due to GAA configuration leakage is further reduced to smaller value.

Oxide layer is the main barrier for electrons in gate and channel region. Potential barrier height is reported to γ = 2.4 eV [17, 18]. At the Si/Sio2 interface therefore qγ energy is required to move the electron from the silicon conduction band to silicon dioxide conduction band. Potential barrier come to be in shape of trapezoidal due to gate oxide voltage drop VOX therefore this voltage drop is defined as

$$V_{OX} = V_{gs} - V_{FB} - \emptyset_S \tag{13}$$

Where Vgs is the gate to source voltage, VFB is the flat band voltage and $\emptyset_S$ is the channel potential at the surface. Tunneling probability confined by trapezoidal potential barrier can be defined by given equation

$$D(E_X) = e^{\frac{-2[2m(E_b - E)]^{1/2} dx}{\hbar}} \tag{14}$$

Figure 4 shows the transfer and output characteristics of GAA n-FET having nanowire diameter of 80nm and channel length (wire length) of 120 nm. Device is achieved lower leakage (off current) of 2.9 uA and higher on drive current of 1.024 mA. Lower tunneling current of 1 mA drives the GAA n-FET at higher value.Subthreshold swing SS is achieved of 46.5 mV/dec.

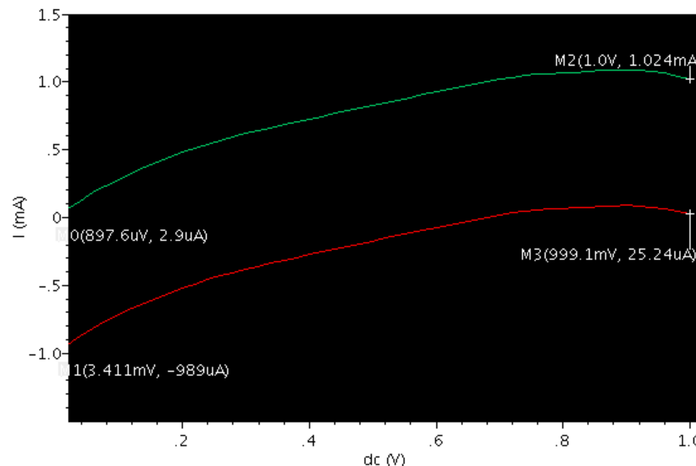

Figure 4.I_D-V_{DS} output characteristics curve

Sub-threshold is usually operated under weak inversion where the surface potential due to channel become constant across the channel and the current flow is mainly depended on diffusion of minority carriers that occurs by lateral concentration gradient effect. The sub-

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threshold slope factor n can be evaluated by gate and bulk capacitances Cg and Cb of FET respectively that is shown below.

$$n = 1 + \frac{C_b}{C_g} \tag{15}$$

The sub-threshold swing can be calculated by expression which is shown below

$$S = n.V_T.\ln(10) \tag{16}$$

As increase tunneling voltage electron tunneling enhances that reduce the gate capacitance therefore sub-threshold factor n increases considerably that further increase the sub-threshold slope. Subthreshold slope SS is limited to under 50 mV/decade by thermionic emission-diffusion carrier effect but the tunneling mechanism does not rely on the same concept. Tunneling junction model is derived by band to band tunneling current which is given by

$$I = aV_{TN} \in e^{-\frac{b}{€}} \tag{17}$$

Where a and b is defined as

$$a = Aq^3 \frac{\sqrt{\frac{2m}{E_g}}}{4\pi^2\hbar^2} \tag{18}$$

$$b = 4\frac{\sqrt{mE_g^{3/2}}}{3q\hbar} \tag{19}$$

a and b depended on characteristic property of materials and cross the sectional area of device. € is the electric field at junction of tunneling model VTN.

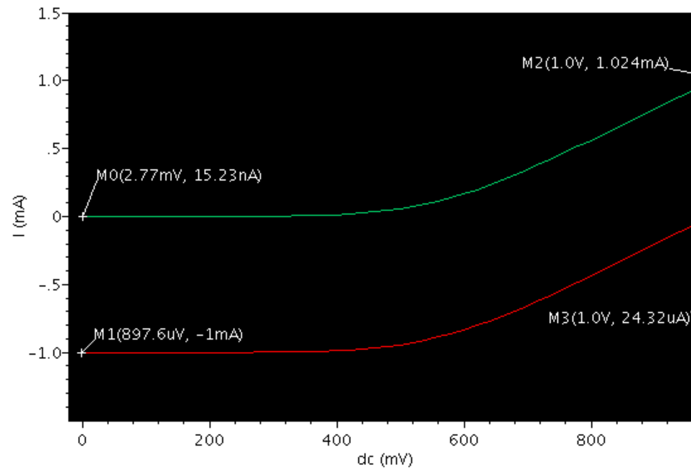

Figure 5. I_D-V_{GS} transfer characteristics curve

3. Analysis and Optimization of Series Resistance R_{SD}

The total on resistance RT of the Gate-all-around FET and GAA with tunneling effect shows in Figure 4. The total resistance of the FET is the combination of series resistance RSD and resistance of channel region RCHANNEL. Series resistance RSD contains the source resistance (RS) and drain resistance (RD) [19]. By applying for tunneling junction model their additional resistance RTUNNEL that is determined by the channel mobility drift mechanism.

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$$R_T = R_{SD} + R_{CHANNEL} \tag{20}$$

$$R_T = R_S + R_D + R_{CHANNEL} \tag{21}$$

$$R_T = R_S + R_D + R_{CHANNEL} + R_{TUNNEL} \tag{22}$$

Tunneling barrier exhibit between source and the channel region is formed by applied for tunneling model is determined by band-to-band tunneling effective mechanism. GAA with tunneling effect having two different regions of operation which depends on both RCHANNEL and RTUNNEL. The band-to-band tunneling mechanism determine the on drive current IDS that is higher when the tunneling effective region is dominated. Drift mechanism determine the on drive current IDS where only RCHANNEL resistance is dominated, ION/IOFF ratio is important factor that depended on series resistance.

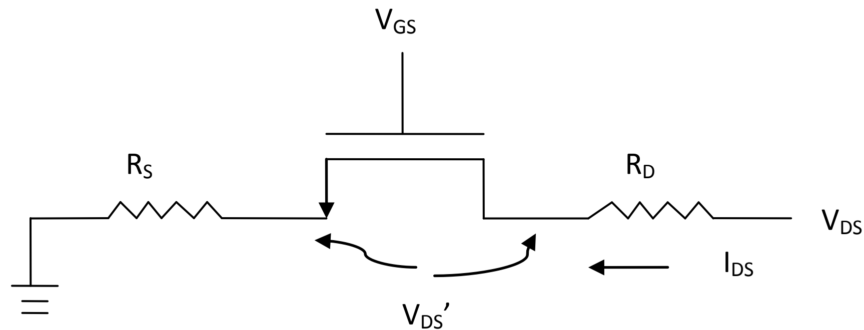

Figure 6(a). Schematic of equivalent GAA nanowire n-FET

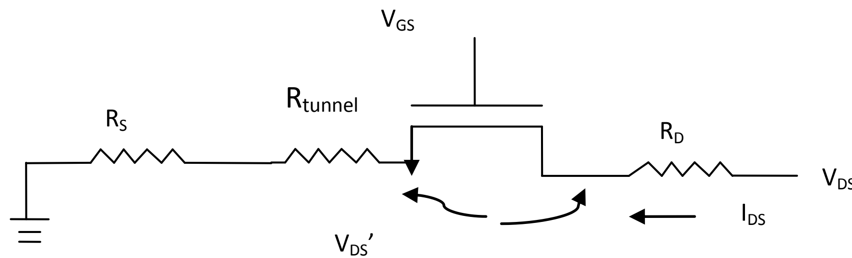

Figure 6(b). Schematic of equivalent GAA nanowire n-FET with tunneling effect

ION/IOFF ratio simply depended on saturation (On current) and Leakage (Off current) whenever this ratio increases then On current driving capability increases usually. Series resistance is depended on channel resistance and source to drain resistance that is shown below by given equation.

$$R_S = R_{SD} + R_{CH} \tag{23}$$

Where RCH can be defined as given below. Here Ids is the saturated On current therefore ION/IOFF ratio is affected by series resistance.

$$R_{CH} = \frac{V_{ds}}{I_{ds}} \tag{24}$$

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Figure 7 shows the mobility degradation effect with operating voltage at gate VGS.This degradation effect occurs due to hot carriers mechanism. In the hot carrier mechanism or effect, carriers are drifted frequently by the electric fields due to the channel and these carriers trapped in the oxide field. These trapped charges shifts parameters threshold voltage VTH that cause degradation effect.GAA nanowire show minimum degradation effect due to lower electric field developed around channel with tunneling voltage and charge carriers is sustained because of gate oxide around four side of gate. Silicon nanowire GAA FET is reported minimum mobility degradation effect with comparison to planar FET due to channel volume inversion [20, 21]. As GAA silicon nanowire is confined to better electrostatic control over channel therefore electron mobility increases significantly but in silicon nanowire mobility degradation is minimum that provide lower volume inversion.GAA nanowire FET with tunneling effect show minimum degradation effect as compared with GAA FET without tunneling effect.

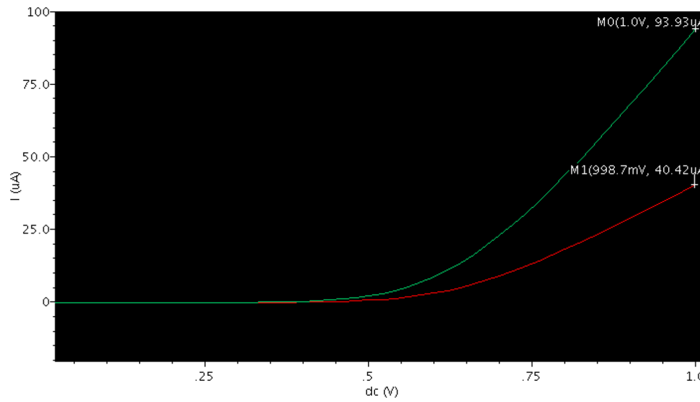

Figure 7. Shows comparison of I_{DS}-V_{GS} characteristics between GAA silicon nanowire FET and GAA silicon nanowire FET with tunneling effect

Y function can be derived as a function of transconductance gm that inherently describe as

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{25}$$

Drain current can be evaluated in linear inversion region. For lower drain voltage VDS, general expressions of IDS is given as

$$I_{DS} = X0 \times V_{GSEFF} \times V'_{DS} \tag{26}$$

$$V'_{DS} \equiv (V'_{DS} - I_{DS} \times R_{SD}) \tag{27}$$

Where VDS is the applied voltage between drain and source end and V'DS is dropped drain voltage over the channel. VGSEFF is the effective gate voltage for charge inversion in channel region. X0 is the considered parameter that depends on device structure. X0 can be evaluated by different manner. Expressions of X0 is described for GAA bulk device structure is given by [22, 23, 24]

$$X0 = \mu_{eff}\, C_{OX} 2\pi\, {}^{R}/_{L} \tag{28}$$

$$X0 = \mu_{eff}\, C_{OX}\, {}^{W}/_{L} \tag{29}$$

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$$X0 = C_{OX} W \vartheta_t \, {}^{(1-r)}\Big/_{2k_B}{}^{t}\!/_{q} \tag{30}$$

Where μ_{eff} is the mobility of charge carriers, COX is the oxide capacitance and the aspect ratio W/L. For ballistic condition r can be defined as resistivity at source node and ϑ_t is thermally accelerated electron behavior with kB is Boltzmann constant. Y function can be evaluated by transconductance gm and drain to source current IDS.

$$Y \equiv \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{X0 \times V'_{DS}} \times (V_{GS} - V_T) \tag{31}$$

Y function value is observed of 1.51 that is smaller value provides the lower leakage current as IDS directly depended on Y value. As smaller value of Y then lower value of off current is reported. Figure 8 shows the Y function value as linear scale with VGS.

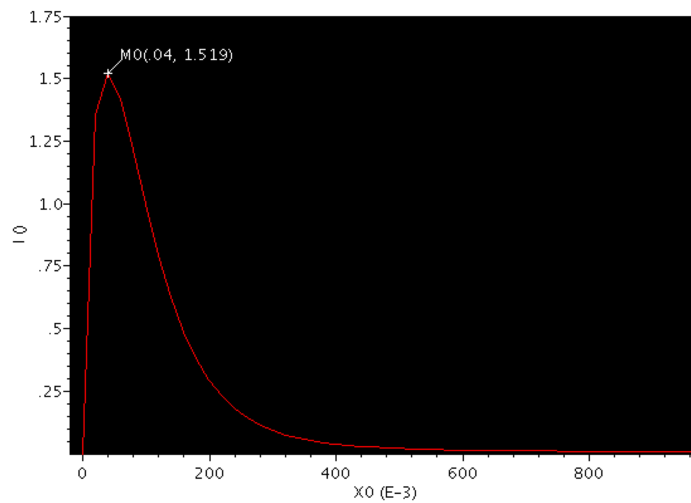

Figure 8. Show Y-V_{GS} characteristics curve

4. Results and Analysis

As increasing tunneling junction voltage then Subthreshold slope increase shows the behavior of tunneling model effect that differs as compared with FET not confined by tunneling effect. Figure 9 emphasizes increase in SS with increase tunneling junction voltage.But after voltage above 2.7 V there is the little dip in SS.

Figure 9 describes the DIBL effect as linearly with the tunneling junction voltage. As increasing tunneling voltage Threshold voltage increases as effective tunneling voltage that enhance DIBL that increases linearly. Equation given below shows tunneling effect increases DIBL.

$$\text{DIBL} = \frac{V_{t1} - V_{t2}}{V_{DS}\,(1V) - V_{DS}(0.1V)} \tag{32}$$

Where Vt1 and Vt2 are the threshold voltage at applied operating voltage VDS of 1 V and 0.1

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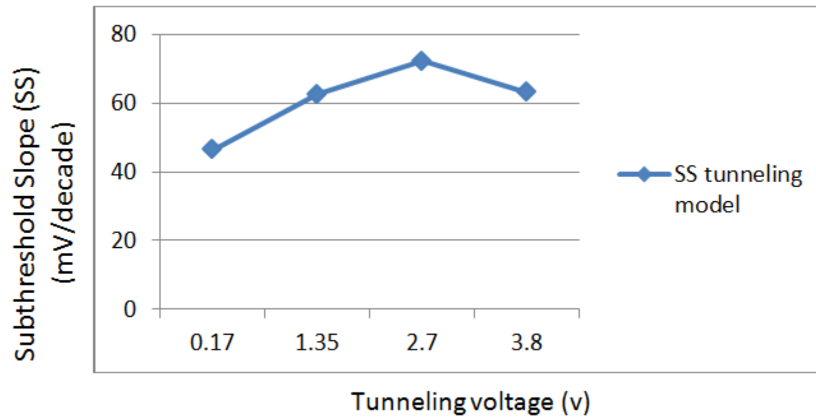

Figure 9. SS-V_{TN} behavior

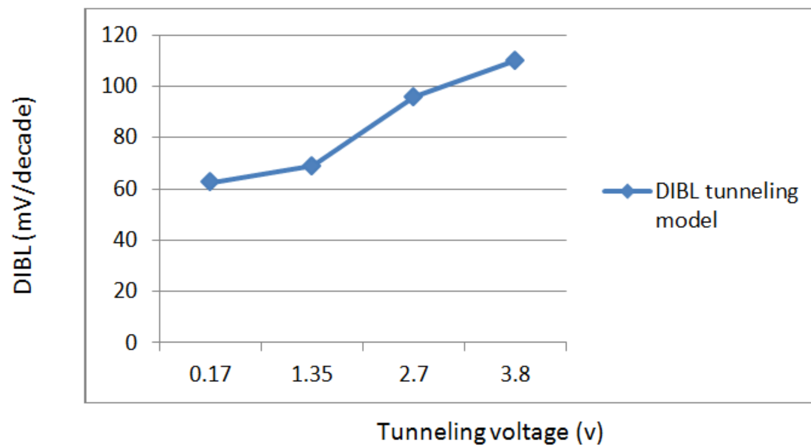

Figure 10. DIBL versus tunneling junction voltage behavior

As gate to source voltage VGS is applied and linearly increasing then Y function value continuously decreases.Y versus VGS behavior showing in Figure 11.

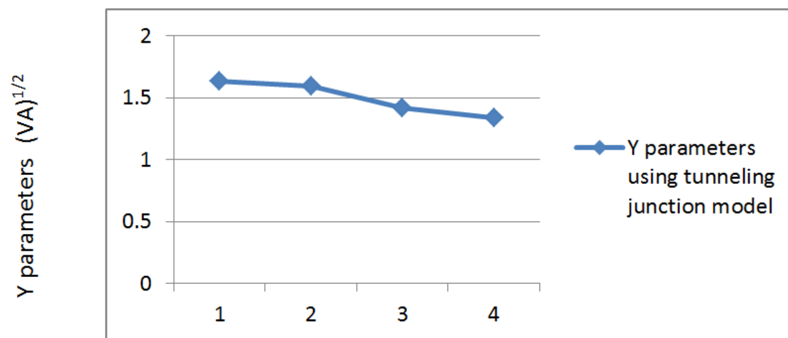

Figure 11.Y function as linearly with gate supply voltage V_{GS}

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Table 1. Comparision of different parameters between GAA nanowire FET and same configuration with tunneling effect

Parameters	GAA nanowire FET with tunneling effect	GAA nanowire FET without tunneling effect
Subthreshold Slope (SS)	46.5 mV/decade	95 mV/decade
Drain induced barrier lowering(DIBL)	62.6 mV/V	64 mV/V
I_{ON}/I_{OFF}	6.7×10^{8}	1.4×10^{5}
Y parameters	1.519	2.234

Table 1 show the effect of tunneling on GAA nanowire FET.SS is lowered to 46.5mV/decade as compared with the same configuration without tunneling. There is a little dip into DIBL with tunneling effect. ION/IOFF is achieved of 108 values which show the lower leakage current. An optimization of series resistance RSD is evaluated by Y function is lowered value of 1.519 as compared without tunneling effect.

5. Conclusion

This paper is presented the silicon nanowire n-FET with tunneling effect by tunneling junction model with subthreshold slope SS of 46.5 mV/decade. Higher ION/IOFF of 108 is achieved that enhance ON drive current. This model provides the substantial work for silicon nanowire GAA FET that is acceptable as a promising candidate for future electronics devices. This can be enhancement in ON current. Optimization of series resistance that has been extracted by using Y function. RSD is calculated is extracted flatten over entire range of gate voltage applied.It is mainly applicable to silicon nanowire FET because mobility degradation effect is suppressed.

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Authors

Awanit Sharma was born in 8th Jan 1984.He received the Bachelor degree in Electronics and Communication Engineering from RGPV University, India and he is pursuing Master degree (VLSI) from ITM Gwalior, India. His current research interest include are VLSI design, Low power design, noise modeling of nanoscale semiconductor devices.

Shyam Akashe was born in 22nd May 1976. He received his M.Tech from ITM, Gwalior in 2006. He is currently working as Associate Professor in Electronics Instrumentation Engineering Department of Institute of Technology Management, Gwalior. Currently, He is pursuing his Ph.D from Thapar University, Patiala on the topic of Low Power Memory Cell Design. His research interests are VLSI Design, Low Power, VLSI signal processing, FPGA Design and Communication System.

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