International Journal of Advanced Science and Technology
Vol.58, (2013), pp.87-102
http://dx.doi.org/10.14257/ijast.2013.58.08

Design and Investigative Aspects of RF-Low Power 0.18-µm based CMOS Differential Ring Oscillator

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Abstract

This manuscript presents the designing and investigative aspects of a low power, wide frequency range, and delay cell based 3 and 5-stage ring oscillator for RF-Ultra-Wide-Band application. The wide range of frequency is achieved by using two variable voltage sources i.e. control voltage source (V_{cntrl}) and tail current source (V_{tail}). A tail current improvement is responsible to control the charging and discharging time of oscillator. Moreover, the push-pull configuration is also used to attain high frequency. In addition, the proposed work presents the effect of control voltage and tail current source on the oscillator frequency. This work establishes a relation between oscillator frequency and its power consumption. This work also gives a comparison between 3-stage and 5-stage ring oscillator. The circuit is implemented in 180 nm CMOS process provided by TSMC. The designed oscillator is measured to cover a frequency range of 1.3 – 5.7 GHz for 3-stage and 1.99 – 3.12 GHz for 5-stage ring oscillator. The simulated circuit draws 0.510 mW of average power for 3-stage ring oscillator and 0.719 mW average power for 5-stage ring oscillator.

Keywords: *CMOS, low power, phase noise, differential delay cell, and voltage controlled oscillator (VCO)*

1. Introduction

Nowadays short-range wide bandwidth communication systems are used by the ultra wide band (UWB) technology. The design and implementation of integrated high speed communication system exhibit many challenges such as declining power consumption while maintaining the speed and the bit error rate (BER) of the system [21]. Since Phase Lock Loop (PLL) is the most important component for any UWB system [13]. And the tuning range as well as power consumption of a PLL is controlled by Voltage Controlled Oscillator (VCO). So, VCO is the most decisive component for a PLL [4]. All modern communication system requires a stable periodic signal to provide the timing basis for functions such as sampling, synchronization, frequency synthesis *etc.* [21]. This periodic signal acknowledged as clock is generated within the system by integrated oscillator. The design of the VCO has to face many challenges like; it is tough to design a wide frequency tuning range VCO with the shrinking size of technological features, which induce lower supply voltage and maintain acceptable power consumption, however, it is very crucial to some applications. A good VCO should have major factors such as high frequency range with lower power consumption.

The VCOs can be categorized into two broad categories such as Ring oscillator and LC tank [4]. For better phase-noise and frequency performance, LC tank oscillators are dependent on high quality factor 'Q' of LC resonant networks [4, 21, 23]. As a result, maintenance of power consumption, complexity and eddy currents in the LC oscillator becomes a very difficult task [14, 10]. On the other hand, wide range of frequency and

ISSN: 2005-4238 IJAST

lower power consumption can easily be achieved by ring architecture. This architecture is also commonly used for multiple output phases [10]. As LC counterpart, Ring oscillators occupy less chip area [3, 11, 15]. However, the single loop ring oscillators face some major frequency limitations such as number of stages and each inverter's smallest delay [15].

The proposed prototype is designed in 0.18-µm CMOS technology process provided by TSMC, and achieves maximum oscillation frequencies (F) up to 5.7 GHz with very less power consumption of 0.510 mW. In Section-II, the generic architecture of proposed differential delay cell is discussed. Section-III describes the basic consideration adopted during designing. Section-IV presents performance comparison between 3-stage and 5-stage designed ring oscillator. In Section-V, simulation results are presented. A conclusion is then given in Section-VI.

2. Proposed Ring Oscillator

The differential ring oscillator block diagram as shown in Figure 1 [1] is the modified topology of [1] used in the proposed design. The differential delay cell rejects the common mode and power supply noise and improves the noise performance [12]. The major dissimilarity between single ended and double ended ring oscillator is that, it has two differential inputs as compared to single. In the differential configuration a last differential buffer stage can be added to odd number of delay stages, if the output is not stable, this will create even stages [12].

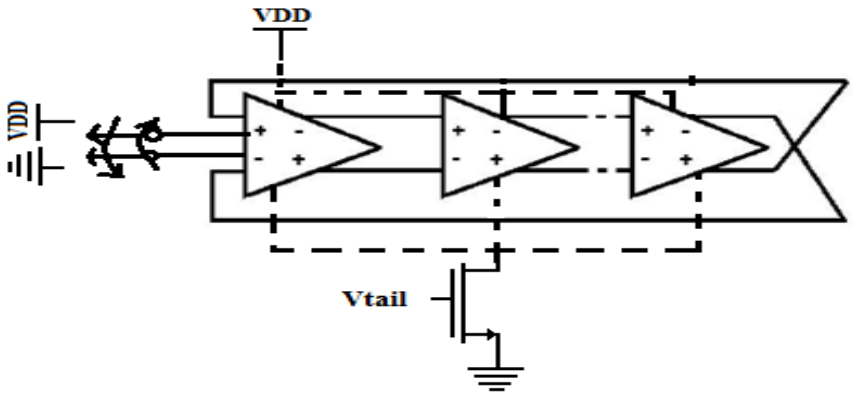


Figure 1. Topology of N-stage Differential Ring Oscillator

In this paper, 3 and 5-stage tail current improved differential voltage controlled ring oscillators (DTVCRO) are designed. It is known that the power consumption will increase as the area and number of stages of the ring oscillator increase. To overcome this problem the proposed ring oscillator is deliberately designed by using least number of transistors as well as stages. The proposed design in Figure 2 shows, the inputs of the delay cell are control voltage (V_{cntrl}) and the output feedback. In Figure 2, transistors M1 & M2 act as differential load and transistors M3 & M4 construct a path from V_{dd} to ground. The combination of M1, M2, M3, and M4 act as NAND gate. Similarly the combination of M1', M2', M3', M4' creates another NAND gate. V_{out+} and V_{out-} are the outputs of this configuration, and are connected with the input of the push-pull inverters in + and in -, respectively. It is well known that if any one input is logically high then the output of the NAND gate is inverted to the second input [22]. In the other words it will act as an inverter. So for the normal operation of the oscillator one input of the NAND gates is always logically kept high. However, for the ideal mode this input of the NAND gate is kept low. This differential mode ring oscillator is designed with two identical NAND gates. To enable the oscillation, out of two inputs of the NAND gates, one of the inputs (V_{cntrl+} and V_{cntrl-}) is connected with logically high, however, the other input (in1+ or in1-

) is connected with the feedback path of the last stage ($V_{out\ n+}$ or $V_{out\ n-}$). Moreover, the transistor M1, M3 and M2, M4 are connected with the same gates of the delay cell. This type of configuration is called as push pull configuration, which is helpful to increase the gain [15]. By this configuration the higher frequency can be achieved easily.

It is known that any changes in the transconductance of the differential pair transistors, leads the changes in gain of the system that shifts the output of common mode levels from low to high values, due to which the output is clipped off [12]. This adds the nonlinearity in the system. To avoid this condition in the proposed design the tail current source transistor M5 is added, which helps to suppress common mode levels variation.

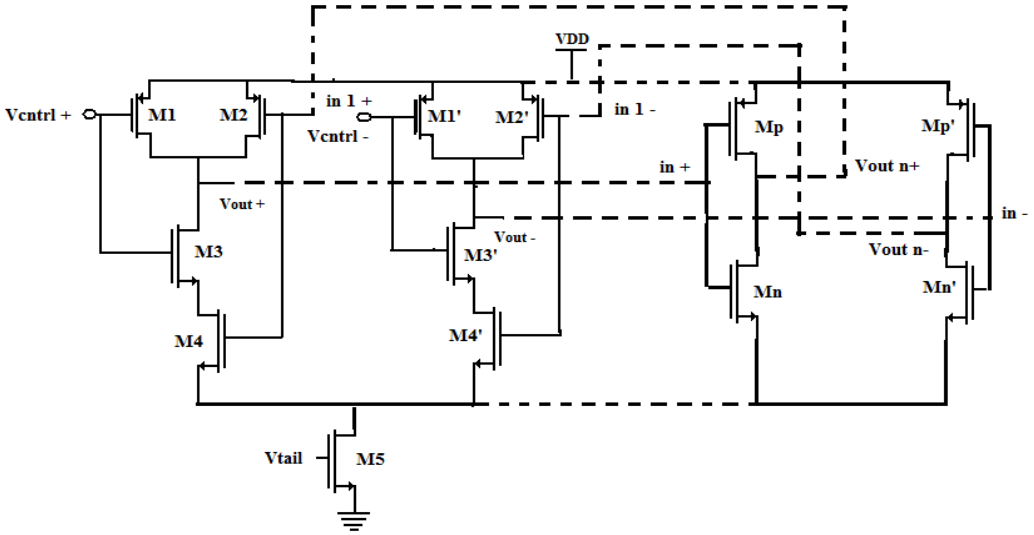


Figure 2. Proposed Delay cell DTVCRO

3. Design Consideration

This section gives a basic idea, different challenges and design consideration adopted during the designing of the proposed ring oscillator. This section also relates the different parameters with each other during the designing phase.

3.1. Frequency Related Issues: As shown in Figure 1 and 2, each delay cell has an 'inverter pair delay'. This is defined as the sum of the rise and fall time of an individual inverted stage [1], *i.e.*, for N-stage ring oscillator the oscillation frequency is defined as [1]:

$$F_{osc} = \frac{1}{N\,(\tau_{rise} + \tau_{fall})} \quad (1)$$

Where, F_{osc} is the frequency of oscillation, N is number of stages, and τ_{rise}, τ_{fall} are the rise and fall time of each delay stage respectively. Now consider the ideal ring oscillator. Thus by taking $\tau_{rise} = \tau_{fall} = \tau$, the frequency of oscillation is defined as [1, 11]:

$$F_{osc} = \frac{1}{2N\tau}$$

As 3 and 5-stage ring oscillators are presented in this paper by putting N = 3 and 5, the frequency of oscillation is given as $F_{osc} = \frac{1}{6\tau}, \frac{1}{10\tau}$ respectively (2)

The expression (2) is the time domain analysis of ring oscillator. This expression confirms that the ring oscillator oscillation frequency depends on number of stages (N). If

the numbers of stages are more the overall delay increases, which results in diminishing of the frequency of overall system. In other words this expression conveys a relation between oscillator frequency and stages delay. Actually, there is a trade-off between number of stages and frequency of the oscillator. So for high frequency applications it is necessary to design such type of oscillator which has minimum number of stages. Now, let us consider the frequency domain analysis of a single ended ring oscillator, here the oscillation frequency is [21]:

$$\omega = \frac{\tan(\theta)}{RC} \tag{3}$$

Where RC is due to each stage delay and θ is phase shift due to RC delay. According to the Barkhussan criteria, in order to satisfy the oscillation condition, total phase shift of the oscillator around the loop must be equal to a multiple of 2π and each stage of the delay cell has to provide π / N phase shift i.e. for a 3-stage ring oscillator the total phase shift is $\theta = \pi/3$ so the angular frequency reduces to [21]

$$\omega = \frac{\sqrt{3}}{RC} \tag{4}$$

Equation (4) again confirms that there is a trade-off between frequency and stage delay. This relation is verified experimentally in section IV as well. During the designing of the proposed ring oscillator this frequency limitation issue plays a major role. The proposed ring oscillator is designed in such a way that it overcomes the above mentioned limitations.

3.2. W/L Related Issues: Now consider the W/L aspects for the proposed design. For a simple CMOS inverter the (W/L) ratios of the transistors (nMOS and pMOS) are defined as $(W/L)_n$ and $(W/L)_p$ respectively and the total load capacitance is defined as C_{load} [2].

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau_{fall}\,\mu_n\,C_{ox}\left(V_{DD} - V_{t,n}\right)}\left[\frac{2\,V_{t,n}}{V_{DD} - V_{t,n}} + \ln\left(\frac{4\left(V_{DD} - V_{t,n}\right)}{V_{DD}} - 1\right)\right] \tag{5}$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau_{rise}\,\mu_p\,C_{ox}\left(V_{DD} - |V_{t,p}|\right)}\left[\frac{2\,|V_{t,p}|}{V_{DD} - |V_{t,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{t,p}|\right)}{V_{DD}} - 1\right)\right] \tag{6}$$

Where C_{load} is the output load capacitance and C_{ox} is the gate oxide capacitance per unit area. For an ideal VCO $\tau_{rise} = \tau_{fall} = \tau$, the eq. (5) and (6) will be rewritten in eq. (7) and (8). Since the mobility of electron (μ_n) is greater than the mobility of holes (μ_p) ($\mu_p < \mu_n$), so in the proposed design the chosen value of $(W/L)_n$ will be greater than $(W/L)_p$ to improve the frequency range. Equation (7) and (8) show another important consideration of the design that the (W/L) ratio of both PMOS and NMOS transistors are directly proportional to the load capacitance C_{load} and load capacitance is inversely proportional to the angular frequency ω in (3).

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau\,\mu_n\,C_{ox}\left(V_{DD} - V_{t,n}\right)}\left[\frac{2\,V_{t,n}}{V_{DD} - V_{t,n}} + \ln\left(\frac{4\left(V_{DD} - V_{t,n}\right)}{V_{DD}} - 1\right)\right] \tag{7}$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau\,\mu_p\,C_{ox}\left(V_{DD} - |V_{t,p}|\right)}\left[\frac{2\,|V_{t,p}|}{V_{DD} - |V_{t,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{t,p}|\right)}{V_{DD}} - 1\right)\right] \tag{8}$$

This statement gives a relationship between $(W/L)_{n,p}$ and angular frequency ω. Actually based on (3), (7) and (8) it is clearly seen that there is a trade-off between (W/L) and frequency of the oscillation. To avoid this in the proposed design the W/L ratio of transistor is kept in the reasonable range. This consideration is valid for the oscillator only if the other parameters of the abovementioned equation are fixed.

3.3. Power Related Issues: As the low power consumption based devices are more reliable [17], power consumption plays a significant role in CMOS design. Power consumption is reduced by proper selection of logic and architecture. Power consumption of CMOS device depends on several factors such as input voltage, density of circuit, operating frequencies, output loadings and capacitances of device. Power consumption is measured using supply voltages, currents in device, selection of device and operating frequency [18]. The estimation of power in CMOS circuit is classified into two types, static power consumption and dynamic power consumption [16]. Static power consumption is defined as a current path that exists between rails i.e. supply to the ground. Static power consumption calculation exclusively for the leakage current is very small and negligible as compared to dynamic power consumption [2]. However, the dynamic power consumption occurs due to the short circuit currents and switching currents. Short circuit currents are also called crow bar current, as the dynamical changes of each node in circuit changes to maximum of q_{max} to zero [19,20]. The average power dissipation in an N-stage CMOS ring oscillator circuit is [2, 20]

$$P_{avg} = nV_{DD}I_{avg}$$
$$= nNV_{DD}q_{max}f_{osc}$$
Where q_{max}=$C_{tot} * V_{DD}$
$$I_{avg} = NC_{tot}V_{DD}f_{osc} \quad (9)$$

The above equation (9) clearly gives the information that when circuit switches at high frequency the contribution of dynamic power consumption is more due to output load capacitance charging and discharging mechanisms. Where P_{avg} is average power, C_{load} is output load capacitance, V_{DD} is supply voltage and F_{osc} is frequency of oscillation. The power expression given by (9) is valid for any CMOS circuit when the leakage power is neglected and total parasitic capacitance in the circuit can be lumped at the output node with reasonable accuracy with ideal output swing. From equation (9) it is clear that the power mainly depends on C_{load}, F_{osc}. Further by relating the equation no (9), (7) and (8) it can be concluded that power is directly proportional to the load capacitance, which means, if the load capacitance is less then power consumption will be less. However, load capacitance is directly proportional to the transistor size [eq. (7), (8)]. Thus by maintaining the minimum size of the transistor the minimum power consumption can be achieved easily. In the proposed ring oscillator design to diminish the power this consideration is adopted. With the help of equation (9) another relation is obtained that power is proportional to angular frequency also. However by comparing the equation (7), (8) and (3) a relation is established that the highest frequency is achieved by using minimum load capacitance. Finally by combining the eq. (3), (7), (8) and (9) one observation is obtained between oscillation frequency and the power consumption that there is a trade-off between oscillation frequency and power consumption. If the oscillation frequency increases the power consumption will also increase. This relation is verified experimentally in section IV also.

This is the most challenging task for the designers these days that how the power will be minimized for high frequency. This problem is solved in the proposed design by minimizing the number of transistors with minimum (W/L), parasitic capacitance and

number of delay cells. This technique is beneficial for both high frequency operations and low power consumption.

4. Performance Comparisons between proposed 3 and 5-Stage DTVCRO

This section gives a comparison between proposed 3-stage and 5-stage DTVCRO. This section also gives the experimental verification of the statements as used in the previous sections *i.e.*, relation between power and frequency, frequency and control voltages and the relation between frequency and delay stages. All experimental results are plotted in cadence Virtuoso.

Figure 3 and 4 show the experimental graphs of the proposed designs between power (µW) and frequency (GHz) for proposed 3-stage and 5-stage DTVCRO respectively. With the help of these two figures, two relations are established. First, the relation between frequency and the power dissipation of the oscillator and second, the relation between power and number of delay cell used in the oscillator.

Case 1: Power vs Frequency Relation: Here it is clearly seen that in the proposed design, since the frequency increases, the power dissipation of the oscillator also increases. This result easily concludes that the oscillator power is directly proportional to the frequency.

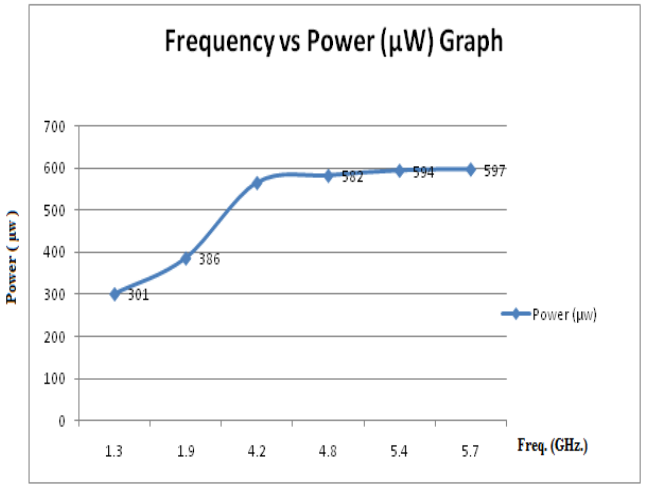


Figure 3. Frequency vs Power Graph for 3-stage DTVCRO

Case II: Power vs Delay Stages: Figure 3 and 4 also establish a relation between power and number of delay stages used in the design. After comparing both the figures it is observed that, the power dissipation depends on the number of stages or number of transistors used in the design. Somewhat similar type of relation between power consumption and delay stages is also describe in [24]. It is clearly seen that the power dissipation is very much low in 3-stage DTVCRO as compared to 5-stage DTVCRO, whereas the oscillation frequency of the 3-stage DTVCRO is high. This is because the numbers of delay cell used in the 5-stage design are more than the 3-stage design. Hence 5-stage design consumes more power.

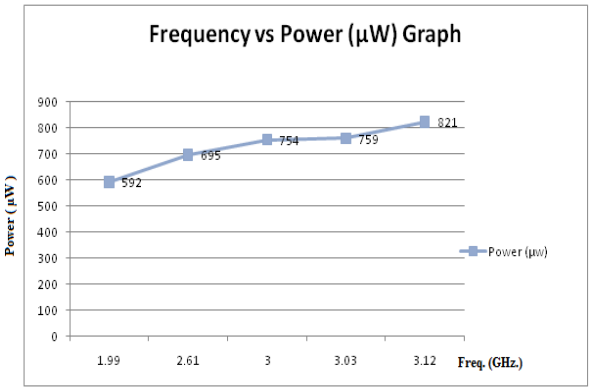


Figure 4. Frequency vs Power Graph for 5-stage DTVCRO

This relation concludes that the power dissipation largely depends on the number of delay stages or transistors used in the design. To overcome this trade off, minimum number of delay cell or transistors based design is beneficial for both high frequency and low power applications.

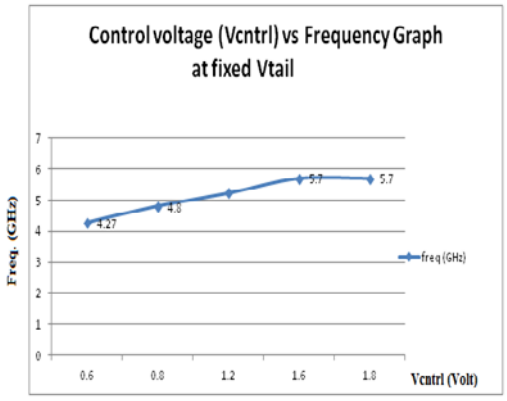


Figure 5. V_{cntrl} vs Frequency Graph for 3-Stage DTVCRO at fixed V_{tail}

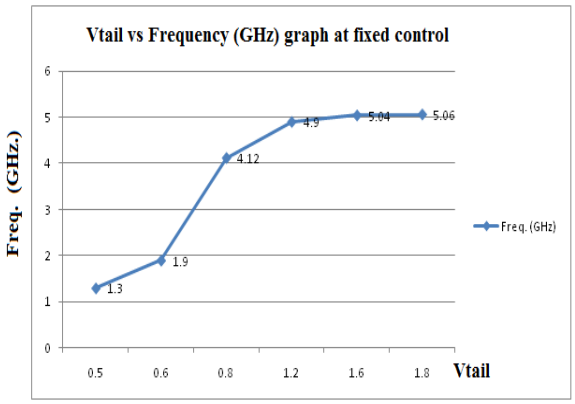


Figure 6. V_{tail} vs Frequency Graph for 3-Stage DTVCRO at fixed V_{cntrl}

Figure 5 shows the experimental graph of proposed 3-stage DTVCRO between control voltage and frequency at fixed tail voltage. It is assumed that the tail current transistor is always in the saturation region. With the help of Figure 5, it is clearly seen that as the control voltage (V_{cntrl}) increases, the output frequency of the proposed oscillator approximately linearly increases upto its maximum 5.7 GHz. Figure 6 shows the graph

between output frequency vs tail voltage (V_{tail}) at fixed control voltage (V_{cntrl}). Here it is clearly seen that after 0.5 V the tail current source transistor starts initial functioning. Between 0.6 V to 1.2 V it will work in triode region as a linear resistor and then shift to the saturation region. The frequency of the oscillation is likely to be constant after 1.6 V.

Similar type approach is used in Figures 7 and 8 for proposed 5-stage DTVCRO design. Here Figure 7 shows the graph between control voltages vs. frequency at fixed tail voltage. In this case, the maximum voltage reaches to 3.08 GHz.

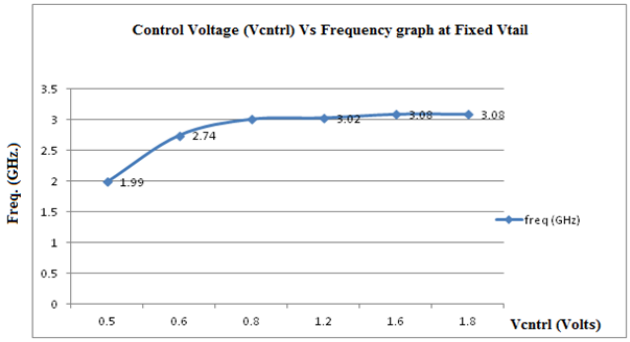


Figure 7. V_{cntrl} vs Frequency graph for 5-Stage DTVCRO at fixed V_{tail}

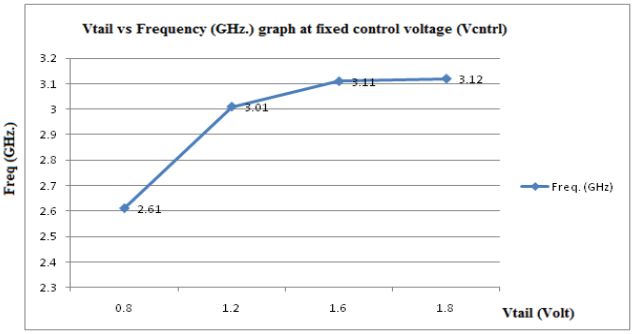


Figure 8. V_{tail} vs Frequency graph for 5-Stage DTVCRO at fixed V_{cntr}

In the proposed design as shown in Figure 2, the oscillator frequency is controlled by two sources *i.e.*, control voltages source (V_{cntrl}) and tail current source (V_{tail}). Figures 5, 6, 7, 8 shows the effect of these two sources on the frequency of the oscillator. Actually this topology is beneficial to achieve the wide frequency range of operation of the oscillator.

Figures 9 shows the frequency range comparison of the proposed 3-stage and 5-stage DTVCRO. The 3-stage DTVCRO maintains 1.3 to 5.7 GHz frequency range, while 5-stage has a range of 1.99 to 3.12 GHz, which is quite less than the 3-stage.

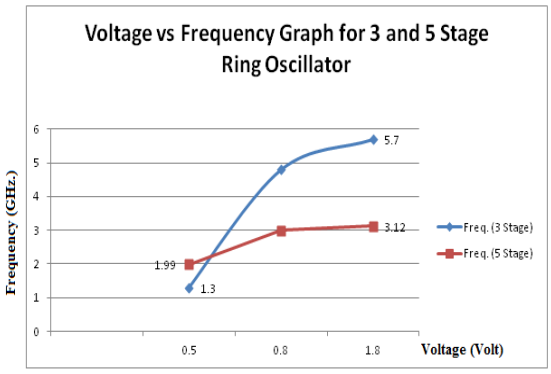


Figure 9. Frequency Variation 3 and 5-stage DTVCRO

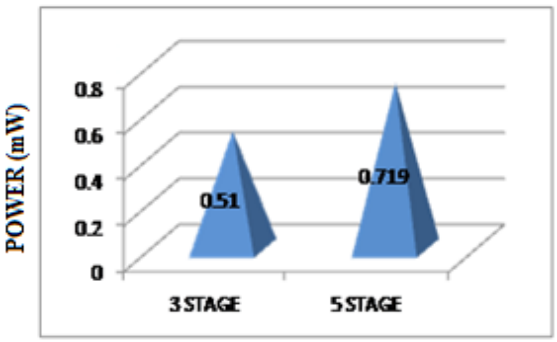
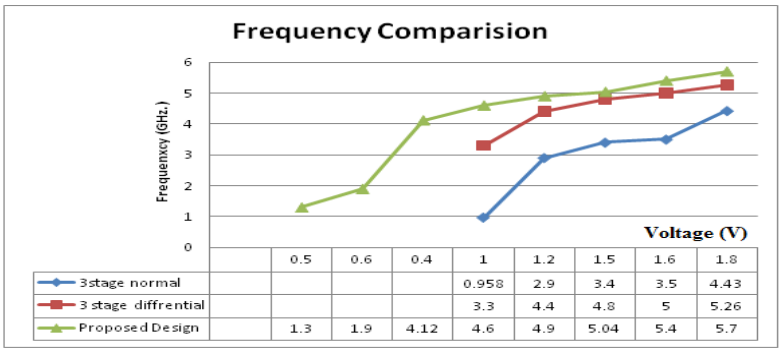


Figure 10. Power Variation in 3 and 5-stage DTVCRO

The graph shown in Figure 9 confirms that as the number of delay stages increases, the frequency decreases. Therefore, it is concluded that the number of delay stages and RC capacitance will affect the frequency of operation of the ring oscillator. Figure 10 shows the comparison graph between power dissipation of proposed 3-stage and 5-stage DTVCRO. With the help of this comparison graph it can be easily concluded that the power dissipation is less in 3-stage DTVCRO due to less number of transistors used. Figure 11 shows the graph of variation in frequency by using different architectures.



	0.5	0.6	0.4	1	1.2	1.5	1.6	1.8
3stage normal				0.958	2.9	3.4	3.5	4.43
3 stage diffrential				3.3	4.4	4.8	5	5.26
Proposed Design	1.3	1.9	4.12	4.6	4.9	5.04	5.4	5.7

Figure 11. Frequency Variation in Different Architecture

5. Simulation Results

This DTVCRO is designed and optimized with Cadence Virtuoso, using 0.18µm 1P6M CMOS technology provided by TSMC and the output responses are plotted using Cadence Spectra.

Figure 12 and Figure 13 show the transient response of the proposed oscillator. Figure 12 shows the output response of minimum frequency obtained by the proposed 3-stage DTVCRO F_{osc} = 1.9 GHz at V_{ctrl} = 1.8 V and V_{tail} = 0.6 V and Figure 13 shows the transient response at V_{ctrl} = 1.8 V, V_{tail} = 1.8 V with the maximum oscillation frequency of F_{osc} = 5.7 GHz by proposed 3-stage ring oscillator.

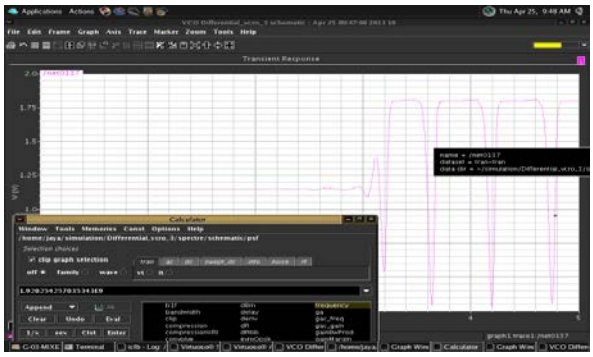


Figure 12. Minimum Oscillation Frequency 1.9 GHz for 3-Stage DTVCRO

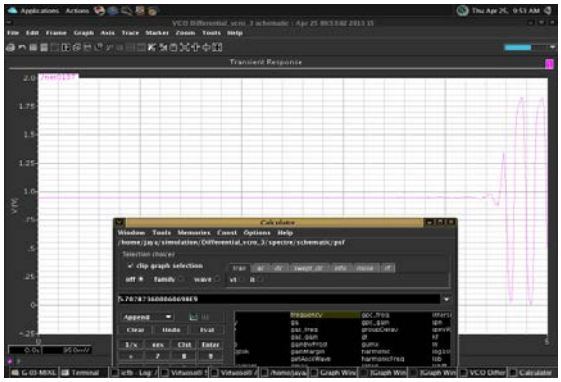


Figure 13. Maximum Oscillation Frequency 5.7 GHz for 3-Stage DTVCRO

Figure 14 and Figure 15 show the transient response of proposed 5-stage ring oscillator. Figure 14 is output response of the minimum oscillating frequency obtained by the 5-stage ring oscillator F_{osc} = 1.9 GHz at V_{ctrl} = 0.5 V and V_{tail} = 1.8 V. However, Figure 15 shows the maximum frequency response by this oscillator F_{osc} = 3.13 GHz at V_{ctrl} = 1.8 V, V_{tail} = 1.8 V.

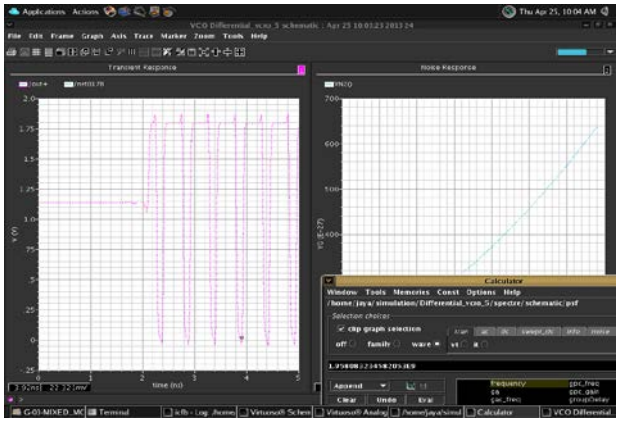


Figure 14. Minimum Oscillation Frequency 1.9 GHz for 5-Stage DTVCRO

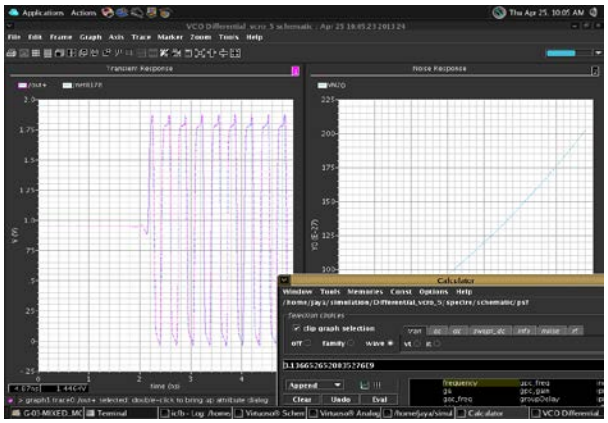


Figure 15. Maximum Oscillation Frequency 3.13 GHz for 5-Stage DTVCRO

Figures 16, 17, 18 and 19 show the average power output response of the proposed ring oscillators. Figure 16 shows the average power of proposed 5-stage ring oscillator P_{avg} = 5.92 µW at minimum oscillating frequency sustained by this oscillator at F_{osc} = 1.99 GHz. However, fig. 17 shows the maximum power dissipated by this oscillator P_{avg} = 8.22 µW at the maximum frequency F_{osc} = 3.13 GHz.

Figure 16. Average Power 5.92 µW at 1.99 GHz for 5- Stage DTVCRO

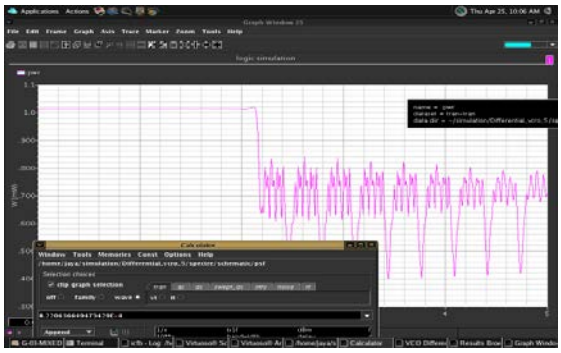


Figure 17. Average Power 8.22 µW at 3.13 GHz for 5- Stage DTVCRO

Similarly Figure 18 and 19 show the average power response of the proposed 3-stage ring oscillator. The Figure 18 shows average power dissipation by the oscillator as 3.86 µW at minimum oscillation frequency F_{osc} = 1.9 GHz.

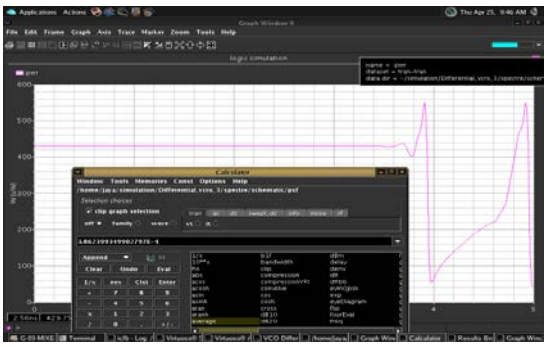


Figure 18. Average power 3.86 µW at 1.9 GHz for 3-Stage DTVCRO

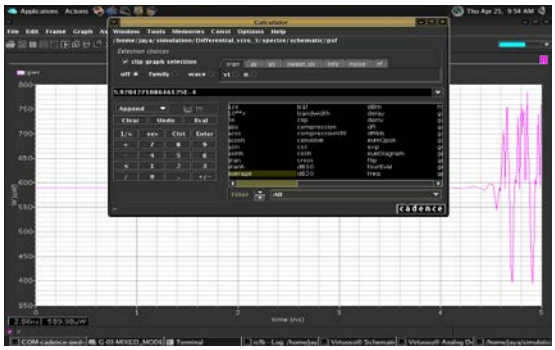


Figure 19. Average Power 5.92 µW at 5.70 GHz for 3-Stage DTVCRO

However, Figure 19 shows the maximum average power dissipation by the proposed oscillator is 5.92 µW at highest oscillation frequency F_{osc} = 5.70 GHz.

Table I. Performance Comparison

Reference	Process Technology(µm)	Type	Tuning Range (GHz)	Power (mW)	Supply Voltage (Volts)
[3]	0.18 CMOS	Ring	1.6	1	1.8
[4]	0.18 CMOS	Ring	3.03-5.36	100	1.8
[5]	0.18 CMOS	Vackar VCO	4.85-4.93	13.5	1.8
[6]	0.18 CMOS	Armstrong VCO	4.96-5.34	3.9	1.8
[7]	0.18 CMOS	Colpitts VCO	4.9-5.46	6.4	1.8
[8]	0.18 CMOS	Hartley VCO	4.02-4.5	6.75	1.8
[9]	0.25 CMOS	LC	4.55-5.45	13.7	1.8
[16]	0.35 CMOS	Ring	450-1150	24.5	3.3
This Work	0.18 CMOS	3-Stage Ring	1.3 - 5.7	0.510 (Average)	1.8
		5-Stage Ring	1.99 – 3.12	0.719 (Average)	

Table I, shows the performance comparison of the proposed ring oscillator in terms of frequency range and power dissipation from other existing designs. With the help of this table it is easily understood that the proposed design has better performance results, in terms of frequency range and power dissipation. If we consider the frequency range, proposed design has wide frequency range. The power dissipation is also very less in the proposed design in comparison to other avilable designs. Figure 20 shows the frequency comparison of the proposed oscillator.

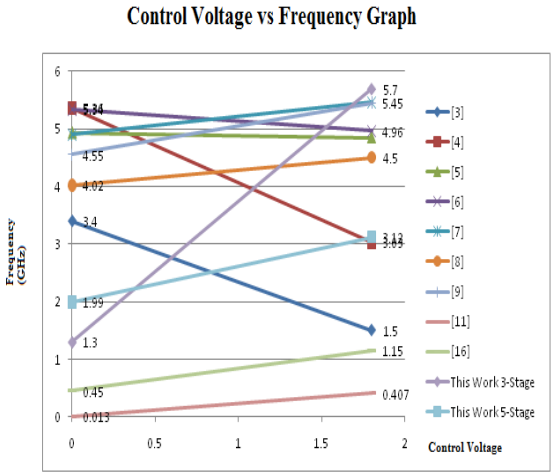


Figure 20. Frequency Performance Comparison

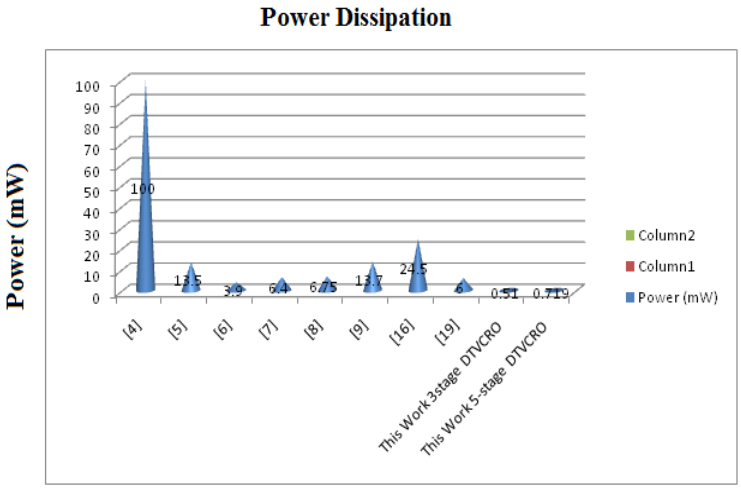


Figure 21. Power Performance Comparison

However, Figure 21 shows the power dissipation comparison of the proposed design with the other existing designs, which shows that the proposed work has the lowest power consumption than the others *i.e.*, 0.510 mW for 3-stage and 0.719 mW for 5-stage. Final layout of the realized 3-stage oscillator is shown in Figure 22.

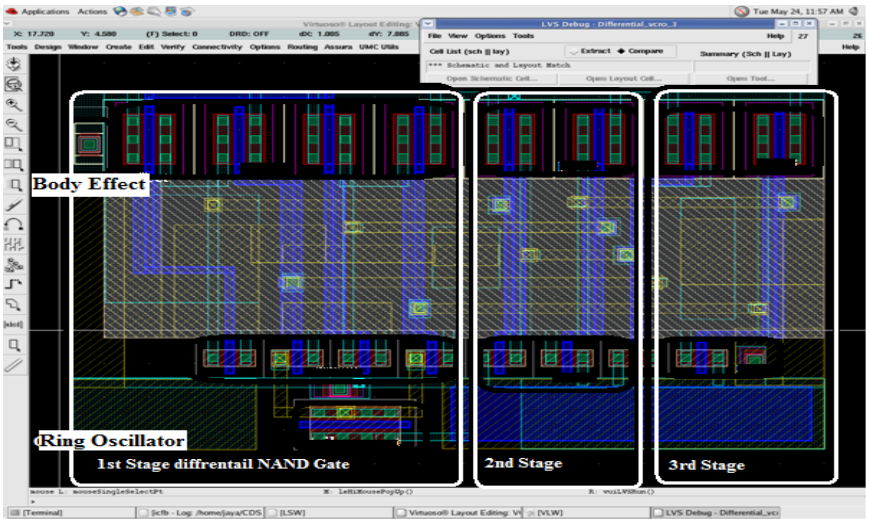


Figure 22. Realized Oscillator

6. Conclusions

In this paper full swing 3-stage and 5-stage DTVCRO architecture is demonstrated and implemented in 0.18 µm technology provided by TSMC. By using two tuning voltage sources (*i.e.*, V_{cntrl} and V_{tail}) and minimum numbers of delay cell the wide range of frequency is achieved. However, low power consumption is achieved by using minimum number of transistors, rail to rail swing and maintaining the minimum W/L. The attractive feature in this paper is to minimize the trade-off between frequency and power. This work gives the various performance curves by which the relation between frequency and power consumption is established. This paper also provides the comparison between 3-stage and 5-stage ring oscillators. The proposed oscillators achieve highest frequency of 5.7 GHz (B.W = 4.4 GHz) at minimum power dissipation 0.510 µW for 3-stage and 3.12 GHz (B.W = 1.13 GHz) at 0.719 µW power dissipation for 5-stage ring oscillator. These characteristics are highly attractive for wireless communication, clock recovery systems, and low power high frequency applications.

Acknowledgement

The authors would like to especially thank and acknowledge the project entitled, “Special Manpower Development Programme (SMDP) – II” funded by Ministry of Communication & Information technology, New Delhi, Government of India, to provide the Cadence software for design and analysis as well as layout of the proposed design and providing technical support for its consummation. We would also like to express our gratitude to the Head of the Department of Electronics and Communication in N.I.T Jalandhar for providing unequivocal support during the different stages of the research work carried out.

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