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Class-AB CMOS Buffer with Low Power and Low Leakage Using Transistor Gating Technique

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Abstract

A rail-to-rail class-AB CMOS buffer amplifier is proposed in this paper to drive large capacitive loads. A new technique is used to reduce the leakage power of class-AB CMOS buffer circuits without affecting dynamic power dissipation .The name of applied technique is TRANSISTOR GATING TECHNIQUE, which gives the high speed buffer with the reduced low power dissipation (1.05%), low leakage and reduced area (2.8%) also. The proposed buffer is simulated at 45nm CMOS technology and the circuit is operated at 3V supply with Cadence software. This analog circuit is performed with reduced performance degradation as well as high current driving capability for the large input voltages. The proposed paper is achieved very high speed with very low propagation delay range i.e.(292×10-12). So the delay of the circuit is reduced to 10%. The settling time of this circuit is reduced by 30% (in ns) at 3V square wave input. The measured quiescent current is 56μA.

Keywords: *CMOS buffer, Class-AB, Rail-to-rail, Settling time, Slew-Rate, Transistor gating technique, Sleep transistor*

1. Introduction

Today CMOS technology has been got more popularity than the bipolar technology especially for analogue circuits in to form the mixed signal systems. The industrial trend of this time wants to achieve the goal of minimum size of the chip. [1] Adel S. Sedra *et al.*, explains that, CMOS also contains the MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The most commonly used as amplifier is common emitter (Bipolar junction transistor) or common source (MOSFET) that magnifies and invert the input signal. [2] Behzad Rajavi says that we know that MOSFET plays an important role in the reduced size of the chip, by reducing the gate oxide thickness of MOSFET *i.e.*, (Tox). But reducing of the Tox gives the reduced tolerance of the MOSFET devices for the higher voltage levels at the gate of MOSFET. It means that to reduce the maximum supply voltages Vdd it gives the helpful purpose. Due to the reduced supply voltages analogue designer have to face some common problems like input common mode range, output swing, and linearity of the device. In the resulting form to implement the desired analogue device we apply the CMOS technology with low voltage and low power techniques.

The second major aspect for the designers of analogue circuits is to stand the circuits with low power dissipation, which is helpful to improve the battery life of the electronic devices proposed by J. Huising *et al.*, [3]. As the CMOS technology is scaled down to the nanometers and femtometers the analogue circuitry has to need to maintain its quality of performance for many parameters like device size, bias currents, voltages, parasitic capacitances and the values of supply voltages is given by Y. Taur [4]. This scaled down feature of the CMOS

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technology and the reduced power dissipation is helpful to get the mixed mode type circuits, which is the combination of the analogue circuits and digital circuits.

Op-amps are the basic block of the analogue circuit, which are used in many applications like Digital-to-analog converters, RF receivers and transmitters is given by W. Black *et al.*, in 1980 [5]. Op-amps are desired with some basic requirements such as low voltage supply, low power dissipation, rail-to-rail output swing, high slew rate, reduced settling time with the critical efficiency of power dissipation. These all requirements are necessary for portable electronics devices. As the op-amps, buffer amplifiers are also most important cell of the analogue circuits. [6] G. Rangan *et al.*, say that buffer amplifier also play an important role in operational amplifier. Basically amplifiers are used for the amplification of the signals.

Amplifiers are mainly designed to amplify the input signal for voltage (voltage amplifier), for current (current amplifier) or for both types (power amplifier). An Amplifier performs operation with a single supply (*i.e.*, Vdd and Gnd) or with double sided supply (*i.e.*, Vdd, Vss and Gnd) is given by J. Solomon [7]. For the analogue systems operational amplifier (Op-amp) is a fundamental block. To achieve the high performance of Op-amp, which is based on the analogue circuits we have to consider some basic parameters for any op-amp. [8] E. Bruun says that an Operational amplifier has many basic parameters in 1994. Some important parameters are given here such as slew rate, settling time, common mode range, frequency response, input offset voltage. These all parameters play an important role for any electronic circuit which is made up with the Opamp.

Class-AB buffer is also described already in background part. Class-AB buffer amplifiers are mostly used by MOS analogue circuitry. Class-AB amplifiers are mainly used for low power consumption and to gain reduced cross-over distortion. Chutham Sawigun *et al.*, proposed paper "A compact rail-to-rail class-AB CMOS buffer with slew rate enhancement" in 2012 [9]. Two prior-art transconductance are used by this class-AB analogue buffer, where DFVF transconductors (Differential flipped voltage follower) is used as basic circuit cell in the buffer design.

The proposed paper is based on the [9] which is proposed with new current leakage scheme. Buffer circuits are mostly used to run the large capacitive load at high speed. Here rail to rail class-AB CMOS buffer is presented to drive the large capacitive loads. Presented paper has the enhanced slew rate with the low power dissipation. This paper is based on the new leakage current technique *i.e.*, TRANSISTOR GATING [10]. In the next section class-AB voltage buffer with its performance analysis is presented. Section III presents the new low power dissipation scheme. Section IV presents the proposed new high speed buffer. Section V has the simulation results of proposed buffer. And Section VI presents the conclusion of proposed buffer.

2. Class-AB Rail-to-Rail Buffer

Class-AB rail-to-rail buffer contains some common features are explained in the following sub-sections.

2.1. Rail-to-rail Input Swing

To achieve the rail-to-rail swing, an NMOS pair and an PMOS pair added in parallel configuration [11].The CMR voltage range of the n-channel pair is written as;

$$V_{cmn} \geq V_{ss} + V_{gsn} + V_{dsn} \quad (1)$$

Where V_{gsn} and V_{dsn} are the gate-source voltage and drain-source voltage respectively. Similarly, the CMR of p-channel pair is written as;

$$V_{cmp} \leq V_{dd} + V_{gsp} + V_{dsp} \quad (2)$$

To get rail-to-rail input range, one or both pair should be in "active mode", which requires

$$V_{cmp-max} \geq V_{cmn-min} \quad (3)$$

Put the equation (1) and (2) in equation (3)

$$V_{dd} - V_{ss} \geq V_{gsp} + V_{dsp} + V_{gsn} + V_{dsn} \geq 2V_{th} \quad (4)$$

Here equation (4) shows that V_{th} of NMOS and PMOS are same, and then the value of applied voltage should be higher than twice of the threshold voltage V_{th} of the applied technology.

2.2. Class-AB Buffer

Class-AB buffer is mostly used to reduce the tradeoff between speed characteristics and power dissipation. The function of class-AB buffer is also called the adaptive biasing [12]. Adaptive biasing is useful to improve the slew rate performance. To achieve this phenomenon we need high quiescent current so, that power -consumption will also increase. To remove this contradiction Transistor gating technique is applied.

In class-AB operation, each device operates the same way as in class-B over half the waveform, but on the same side it also conducts a small amount on the other half. As per result the region where both devices simultaneously are nearly off (the dead zone) is reduced. According to the result when the waveform from the two devices are combined, the crossover greatly minimized or eliminated altogether .The exact choice of quiescent current, the standing current across both devices when there is no signal, then it make a large difference at the level of distortion (and to the risk of thermal run away, that may damage the devices) often the bias voltage applied to set this quiescent current has to be adjusted with the temperature of the output transistor.

2.3. Power Consumption of Circuit

As we know that any CMOS circuit has the power dissipation in the standby mode which is two types static and dynamic dissipation [13]. When the transistors go to switching condition then dynamic power is consumed by the transistors. Some main components of the static power dissipation are given as junction leakage, Sub-threshold leakage, and gate oxide leakage. In the standby mode of the circuit the static power dissipation is given by equation (5)

$$P_l = I_l \times V_{dd} \quad (5)$$

Where P_l is leakage power of the transistor, I_l is leakage current of the transistor in off state of the transistor. And V_{dd} is supply voltage. Here various components are contained by leakage current.

The gate leakage and sub-threshold leakage are main leakage in the given leakages such as sub-threshold leakage, gate leakage, reverse biased junction leakage and gate induced drain leakage.

The sub-threshold leakage current of MOS transistor is given in equation (6) and (7)

$$I_{ds} = I_{dso} e^{\frac{V_{gs}-V_t}{nvT}} \left[1 - e^{-\frac{V_{ds}}{V_T}}\right] \quad (6)$$

$$I_{dso} = \mu_{eff} C_{ox} (W|L) {V_T}^2 \quad (7)$$

Where μ_{eff} is the charge carrier mobility, C_{ox} is the gate capacitance per unit area, W is width and L is length of channel of transistor, V_t is threshold voltage, V_T is the thermal voltage, n is the sub-threshold swing coefficient, V_{gs} is the transistor gate to source voltage and V_{ds} is drain to source voltage.

2.4. Analysis of Settling Time and Slew Rate

To achieve the qualitative and analytical synthesis of any amplifier we have to get the total settling time [14]. Now to determine the basic expression of settling time for any amplifier we will consider the first order model of the amplifier. As we know that any practical system has higher order terms which are comprised by both settling and slewing periods. As shown in Figure (2) we are considering an amplifier with a closed loop and real feedback factor β

Let in the linear region of amplifier the open loop gain AO is much larger than the closed loop frequency gain (1/β). So the time constant τ is given by:

$$\tau = \frac{1}{\beta W_T} \quad (8)$$

Here w_T is the transition angular frequency.

Now we will consider the initial and final values for the step response of this first order system respectively $V_i$and V_f, which is given by:

$$\mathrm{V_o} = (\mathrm{V_f} - \mathrm{V_i}).\left(1 - \mathrm{e}^{\frac{t}{\tau}}\right) + \mathrm{V_i} \quad (9)$$

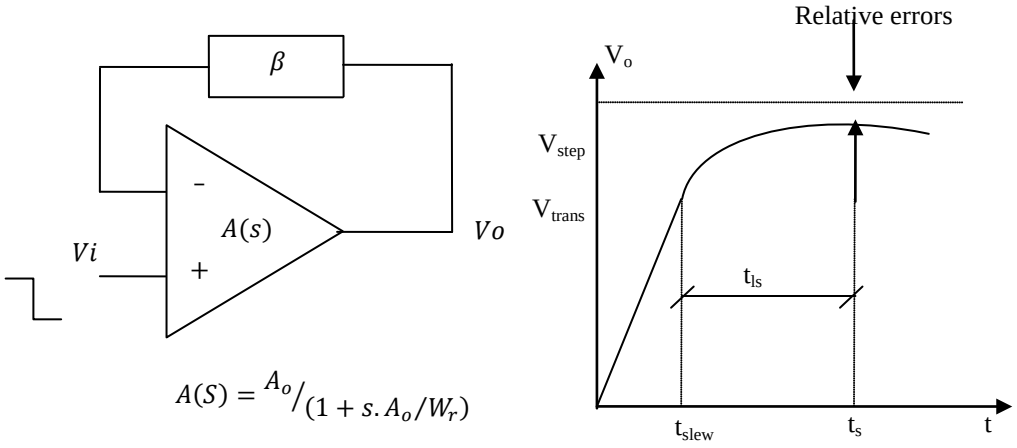

Figure 1. Shows Model for Total Settling Time Analysis

At t=0 its slop will be maximum, which is given by:

$$\frac{dV_o}{dt}|max = \frac{(V_f - V_i)}{\tau} \quad (10)$$

As shown in Figure (1) the first order model is considered for the amplifier, here second stage is performing with frequency independent gain, where at the output of amplifier dynamics that have the imposed slope, at this slope transition occurs, which is given in equation (3) that is called slew rate. Now we can find out the transition at the output voltage.

$$V_o = \frac{(V_{step} - V_{trans})}{\tau} = SR \quad (12)$$

Here $V_f = V_{step}$ that is the amplitude of the output step, $V_{step} = \frac{\text{input step}}{\beta}$

For the total settling time, the dominated part of slew rate is given by:

$$t_{slew} = \begin{cases} \frac{V_{trans}}{SR} = \frac{V_{step} - \tau.SR}{SR} & (V_{step} > \tau.SR) \\ 0 (V_{step} \le \tau.SR) \end{cases} \quad (13)$$

From Figure 2 we can define the linear settling time that takes the output to settle down to $V_{step}$with a relative error of less than ε, then the initial condition V_{trans} is given by:

$$t_{ls} = t \Big/ \frac{|V_o - V_{step}|}{V_{step}} = \epsilon \quad (14)$$

$$t_{ls} = \tau.\left(\ln\left(\frac{1}{\varepsilon}\right) + \ln\left(\frac{\tau.SR}{V_{step}}\right)\right) \quad (15)$$

Where t is time and V_o is output voltage.

Now to get the expression for the total settling time we will add the slewing time and linear time, so that from equation (5) and (7) we will achieve final total settling time.

$$t_s = t_l + t_{slew} = \tau.\left(\ln\left(\frac{1}{\varepsilon}\right) - 1 + \ln\left(\frac{\tau.SR}{V_{step}}\right) + \frac{V_{step}}{\tau.SR}\right) \quad (16)$$

The proposed buffer amplifier has achieved the settling time in nanoseconds is given in Figure 3, which shows that the proposed buffer amplifier has high speed.

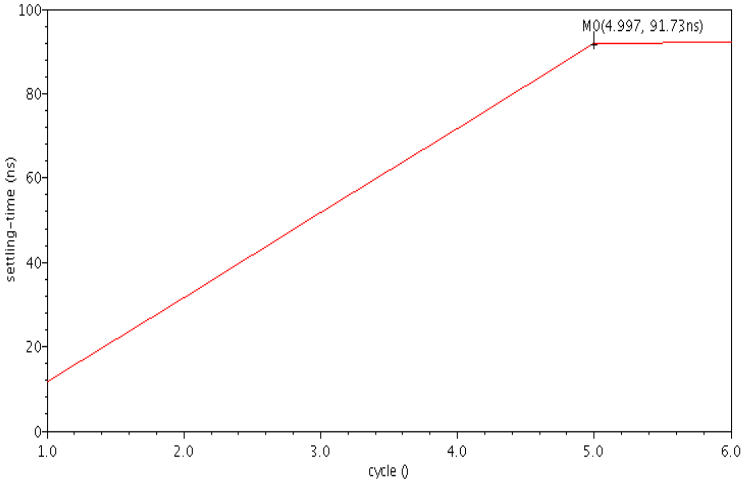

Figure 2. Shows the Settling Time of Proposed Buffer

3. Low Power Dissipation Scheme for CMOS Buffer

We have seen that the buffer's circuit affected by the power dissipation. The power dissipation is an important consideration in the CMOS VLSI design circuits [15]. High power consumption leads to reduction in the battery life-, in the case of battery-powers applications and in reliability, packaging and cooling costs. The main sources of power dissipation are: (a) Capacitive power dissipation. (b) Short circuit currents. (c) Leakage currents. In CMOS technology leakage power occurs due to the sub-threshold which is the reverse current flowing through the off transistor. Gate leakage is also another type of leakage. The feature size and the channel length of transistor are reducing day by day, because the technology is also scaled down. Due to decrement in the channel length we get the increment of the leakage power in the total dissipated power.

From the above theory the gate leakage and sub-threshold are main leakages, that type of leakages can be reduces by help of the TRANSISTOR GATING TECHNIQUE. This technique has two sleep transistor PMOS and NMOS which are used in circuit. Here sleep transistor PMOS (S) is inserted between the pull-up network and network outputs and sleep transistor NMOS (S') is inserted between the pull-down network and ground to reduce the leakage current. During active mode by applying proper gate input voltage both transistor will get on position *i.e.*, high for NMOS and low for PMOS. It is helpful to reduce the resistance of conducting path from power supply to ground, which gives the reduced performance degradation.

During standby mode, by applying proper gate input both sleep transistors will get turn off position *i.e.*, low for NMOS and high for PMOS to produces the stacking effect, which reduce leakage current by increasing resistance of the path from power supply to ground. By help of this phenomenon an additional resistance is provided which decreases the sub-threshold leakage current.

Figure (3) shows the block diagram of TRANSISTOR GATING TECHNIQUE, which has achieve the leakage current of the buffer circuit which is achieved after the simulation of the circuit at cadence software shown in Figure 3. By help of this technique we have achieved the reduced leakage current *i.e.*, 118.4μa and the propagation delay is reduced to picorange *i.e.*, 345.1×10-12.

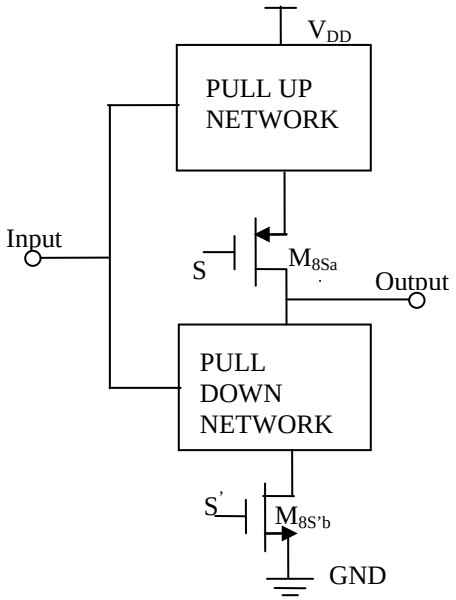

Figure 3. Shows Circuit Diagram of the Applied Technique

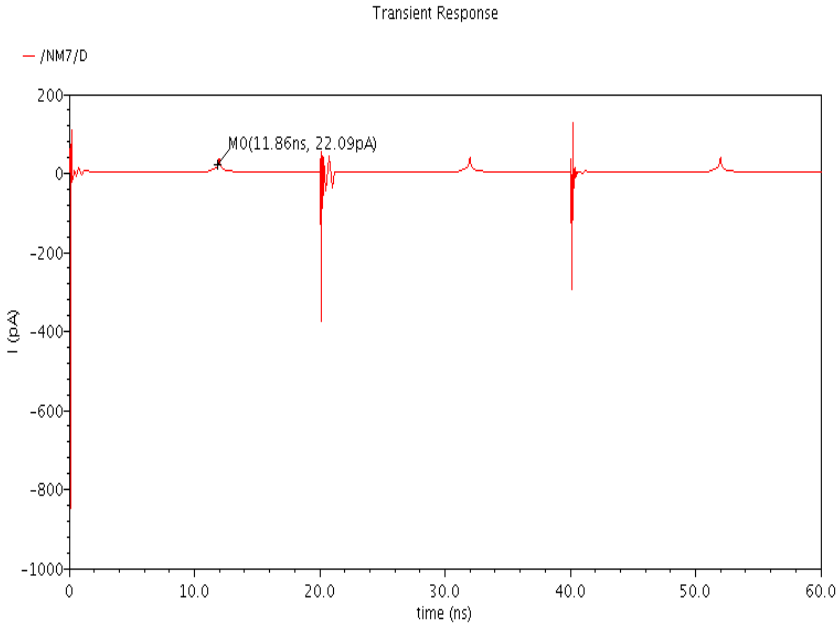

Figure 4. Shows the Leakage Current of the Circuit

As shown in Figure 5, the charging capability of the paper is improved by this paper. Achieved settling time is also improved in this paper. The settling time can be defined as the time required for the output signal reaching within .2% of the output voltage. The simulated settling time is 41.12×10-9s. As shown in Figure 5, $R_{M8s(a|b)}$ and $R_{M7(a|b)}$ are as the channel resistances of the output transistor and the auxiliary driving transistor respectively. Then output response can be written as,

$$V_{out} = V_I + (V_F - V_I)\left[1 - e^{\left(-t/\tau_p\right)}\right] \quad (8)$$

Where V_I and V_F are the initial and final values of the output voltage respectively, and

$$\tau_p = (R_{M8b} \| R_{M7b}) \times C_L \quad (9)$$

$$\left.\frac{dV_{out}}{dt}\right|_{t=t_1} = \frac{(V_F - V_I)}{\tau_p} e^{\left(-t_p/\tau_p\right)} \quad (10)$$

4. New High Speed Buffer with Low Power

Figure 5 shows the proposed class-AB rail-to-rail high speed buffer with low power dissipation. This circuit is divided into two parts: The upper part of the circuit consist transistors Mc1a-c3a with adaptive biasing and added with the transistors M1a-8a. The lower part of the circuit consist the transistors Mc1b-c3b with adaptive biasing and added with M1b-8b. Total stages of the circuit perform as a class-AB amplifier. The level shifters M4a-5a and M4b-5b are used to provide the negative feedback, which extend the input common mode range [16].

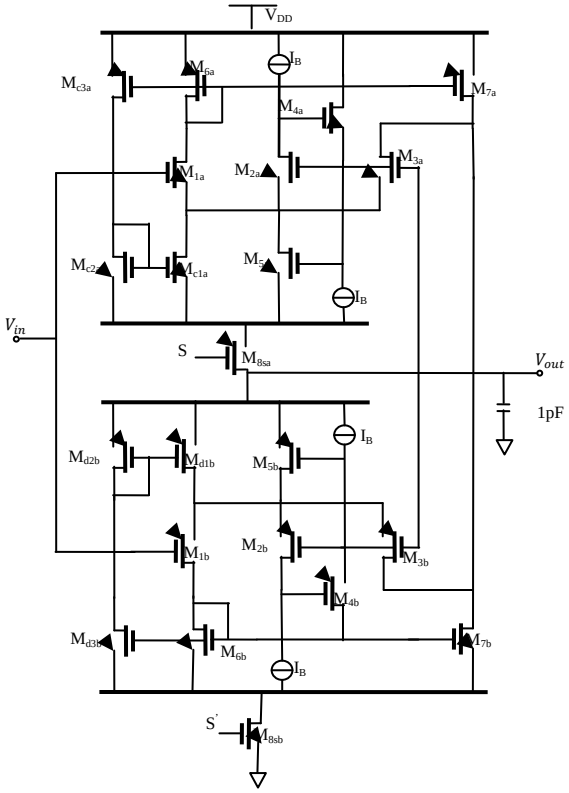

Figure 5. Shows the Schematic of Proposed Buffer

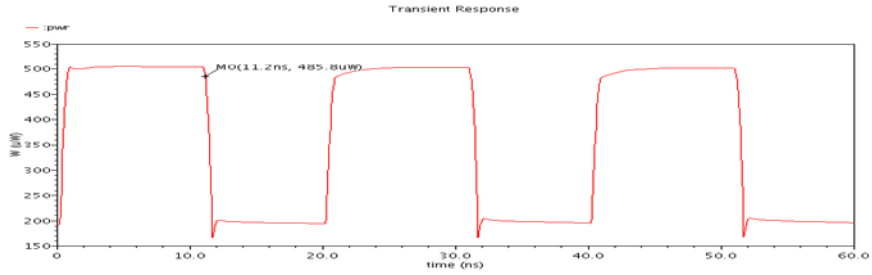

Figure 6. Shows the Power Plot of the Proposed Circuit

The main aim of the negative feedback loop is the low impedances at the source terminals of transistors M2a-2b. This function gives the result in the form of the gate-source voltages of M2a (Vgs2a) and M2b (Vgs2b) are kept nearly constant. This functionality is used to show the class-AB behavior. The inserted transistors M3a-3b are also used to increase the input range, so the gate source voltages of M3a-3b are same as M2a-2b, which gives the same current behavior controlled by V_{in}.Transistors M3a-3b performs the function as the constant controlled sources, which stabilize the DC current of the transistors M7a-7b. The previous paper contains the drawback of power dissipation. Transistors M8sa-8sb is inserted between M7a-7b, these transistors remove the drawback of power dissipation. Function of these transistors is explained in the previous section. The technique is applied on transistors M8a-8b, which is known as TRANSISTOR GATING technique. Figure 7 presents input output

waveform which is achieved from applied new low power dissipation scheme. From this figure we can conclude that this buffer amplifier gives the output same as input with minimum leakage of current.

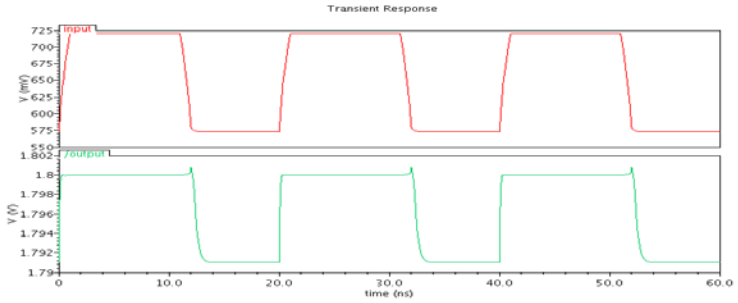

Figure 7. Shows the Input Output Waveform of Proposed Buffer

5. Simulation Results

Using 45nm CMOS technology we designed a new buffer as shown in Figure 5. which is simulated at 3V supply voltage by help of the cadence tool. Figure 5 consists the transistors that all have the same sizing. Bias current I_B is fixed at 10μA in buffer circuit. It contains the 1pF capacitor, fixed at the output side. Table 1 shows the simulation of results, which are giving the overall performance. Figure 6 shows power plot of the output waveform. And Figure 7shows the input output waveform of the buffer circuit. Figure 8 shows the overshoot of the output waveform. Figure.9 shows the period jitter.

Table 1. Simulation Results of proposed Buffer

Parameter	Simulated Results
Process technology	45nm
Power supply	3v
Transistor count	22
Settling time (ns)	34.17×10^{-9}
Overshoot (m^3)	23.21×10^{3}
Rise time (ps)	139×10^{-12}
Slew rate ($^{v}/_{\mu s}$)	90
Period jitter	40×10^{-9}
Phase noise	1.227
Total quiescent current(μA)	41.25×10^{-6}
Propagation delay(ps)	345.1×10^{-12}

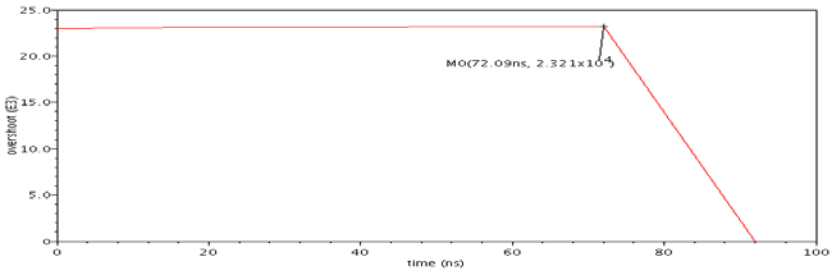

Figure 8. Shows the Overshoot of the Proposed Circuit

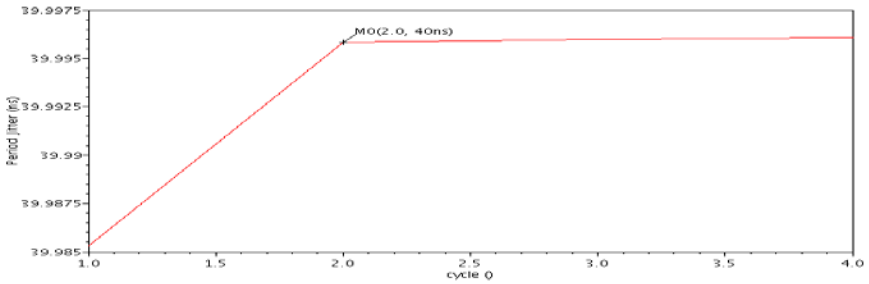

Figure 9. Shows the Period Jitter of Proposed Circuit

6. Conclusion

A new design scheme for CMOS class-AB buffer using the TRANSISTOR GATING technique is proposed. By help of this technique reduced leakage current is achieved. Applying the TRANSISTOR GATING technique with the adaptive biasing into the buffer helped us to get the propagation delay in the range of Pico- seconds i.e.345.1×10-12, from here we can concluded that the speed of this buffer is very high. The settling time of proposed circuit is also reduced to the range of nanoseconds. This technique is also capable to enhance the slew rate, the achieved slew rate is $90(^{V}/_{\mu s})$.The designed buffers is applicable in systems requiring the efficient operation with very low quiescent power consumption.

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