Diode Based Ground Bounce Noise Reduction for 3-Bit Flash Analog to Digital Converter

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Abstract

Flash ADC is an important component for realization of high speed and low power devices in signal processing system .As technology scale down, leakage current becomes the most concerned factor. This paper reports the power gating technique to provide the reduction mechanism for suppressing the leakage current effectively during standby mode but it introduces ground bounce noise. We designed a "3" bit flash ADC with power gating technique to reduce leakage current and ground bounce noise in different mode of operation. This diode based power gating technique provides the reduction of leakage current in standby mode, and reduction of ground bounce noise in sleep-to-active mode. The improved power gating technique provides 82% reduction in leakage current, and 73% reduction in ground bounce noise as compared with conventional flash ADC. Flash ADC with diode based stacking power gating technique has been designed with the help of cadence tool at various supply voltages with 45 nm technology.

Keywords: *Flash ADC, Ground bounce noise, Diode based stacking power gating, Active power, Leakage current*

1. Introduction

ADC is one of the most popular components used in every consumer electronics and computer systems as there rapid incline of electronics system design including communications and signal processing based systems. Flash ADC is mostly used in high speed and low power application [1-4] in recent years system–on-chip grows rapidly therefore signal processing component optimization is an important factor. Analog to digital converters (ADCs) is a mixed signal integrated component that converts analog signals to digital signal; which is the real world signals that has been used for information processing component. The demand of high speed, low operating voltage, low power consumption and the high input signal bandwidth analog-to-digital converter increasing rapidly [5-9].The Comparators are the important component of any flash ADC and performance ADC is strictly depended on comparators .Area, speed and power consumption of computational intensive VLSI systems are well contributed and implemented by flash ADC. Low power and high speed flash ADC is in high demand [10]. The basic technology is defined by making device size smaller one, so it has become difficult to achieve a good tradeoff by device scaling or sizing of the transistors [11]. The gate leakage increases 30 times with new technology [12]. Reducing the leakage, improved design techniques are important. The sleep transistor is connected between the actual ground and circuit ground in the power gating technique [12-13]. To cut the leakage, the path of the sleep mode of this transistor was off. Power gating technique reduces the leakage with minimal impact on the performance of circuit [14] however other power gating

techniques are Multi-threshold CMOS (MTCMOS) [15] and transistor Gating [16].These all reduce leakage current and ground bounce noise .The main focus of this paper is reducing sub-threshold leakage power and ground bounce noise, with the help of a stacking power gating technique

2. Proposed Device Architecture

2.1. Flash ADC

Figure 1 shows block diagram of conventional flash ADC that has been implemented using cadence virtuoso tool with 45 nm technology .We designed 3 bit flash converter in this work. Flash"3" bit converter, simply require 2^3-1= 7 comparators. A resistive divider that incorporated in converter employs 2^3 = 8 resistors for providing the reference voltage in the comparators or converters. Resistive divider provides the reference voltage to each comparator become one LSB (least significant bit) that means it is higher than the reference voltage for the comparator just below the previous one. Each comparator achieves the output "1" whenever input voltage source (analog) V_{in} is higher than the reference voltage Vref provided for comparators .The comparator give output "0"when analog input source becomes lower than reference voltage applied to it.

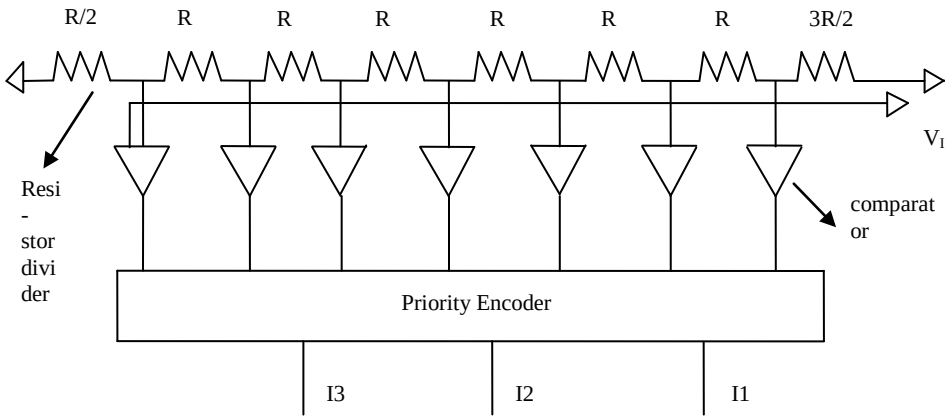


Figure 1. Conventional flash ADC architecture [17]

Each resistor in divider section divides the reference voltage that is applied in upper extreme resistor to feed a comparator. Each comparator achieved the output "1" whenever input voltage source (analog) Vin is higher than the reference voltage Vref provided for comparators. The output of the comparators is not in digital form but there is need to achieve encoded signal, therefore a priority encoder is employed to convert the encoded signal into digital form means "n" bit data format generated in binary code format. Current consumption by the device becomes lower whenever the resistance value getting higher which minimized the power dissipation in the device. Flash ADC "n" bit architecture provides 2^n-1 comparators that consist of differential amplifier based.

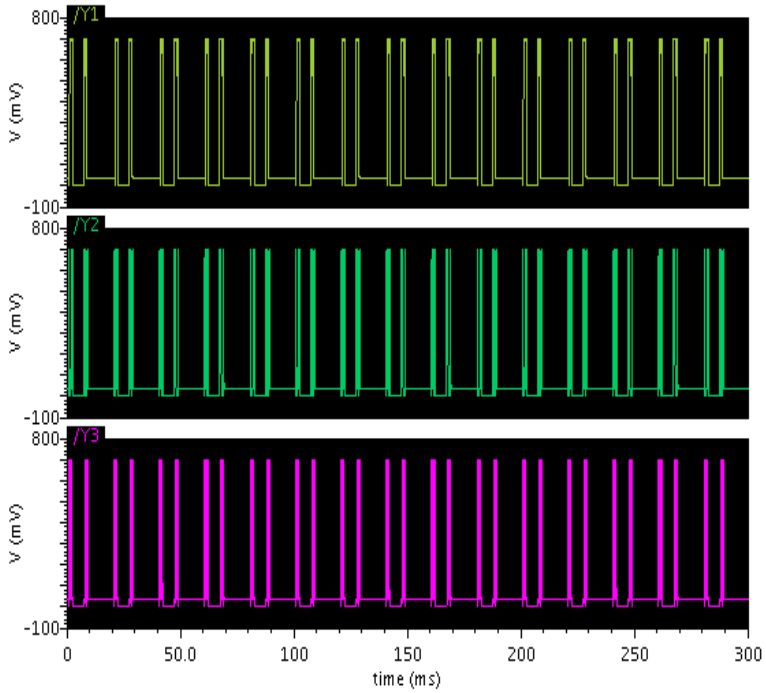


Figure 2.Transient Behaviour of Flash ADC

Figure 2 shows the Flash ADC transient output analysis of "3" bit flash ADC for analog input signal VSIN of 5000 Hz frequency. Bit "0" represent the LSB and bit "2" represent the MSB of the binary digital output of "3" bit flash ADC

2.2. Comparator

Comparator is important component of analog-to-digital converter that plays the important role to achieve overall good performance. It is used in front-end signal processing and electronics components [18] Lowering the input impedance is effective to improve the better performance of comparator [19-22].Inverter based comparator is reducing the offset error [23-24]. Whenever input voltage is just close to reference voltage then it may be high possibility that noise can make the variation of input voltage around reference voltage. This noise can generated output glitches that consume lot of power and provide higher leakage whenever circuit is in standby mode therefore there is need to design a comparator with hysteresis effect to minimize the noise problem and reducing the leakage power.

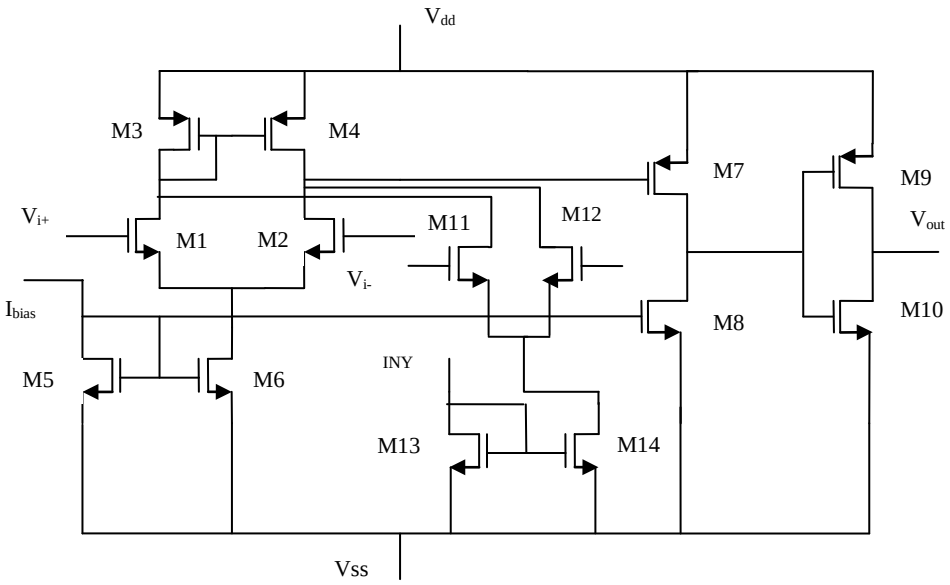


Figure 3. Schematic of Comparator

3. Diode Based Stacking Power Gating Technique

Diode based stacking power gating scheme is an improved power gating technique to reduce the leakage current and ground bounce noise efficiently. The Stacking sleep transistors (ST1 & ST2) are used in this technique as shown in Figure 4. The diode based stacking power gating technique relies on the different component that is described below:

- Transistor ST1 and ST2 are the sleep transistor.
- T3 is the control transistor.
- TG is the transmission gate.
- ΔT is a time delay between T1 and T2.
- C1 is the capacitor.

Whenever the circuit is operated in standby mode, leakage current becomes considerable effect whenever the circuit is doing transition from sleep to active and vice-versa. Ground bounce noise becomes the concerned factor that must be reduce for better operating condition of device. Diode based stacking power technique employ three mechanisms for reducing the current flow through sleep transistor. Diode based stacking power gating technique has three operating modes that are shown below.

3.1. Active Mode

Sleep transistor's ST1 & ST2 always remain in ON condition during the active mode operation and transistor S1 that behave as the control transistor is in OFF condition. ST1 & ST2 both transistors are offer very low resistance level (R1ON & R2ON). C1 is intrinsic capacitance that becomes virtual ground node and C2 is external capacitance become intermediate node between ST1 & ST2 transistors.

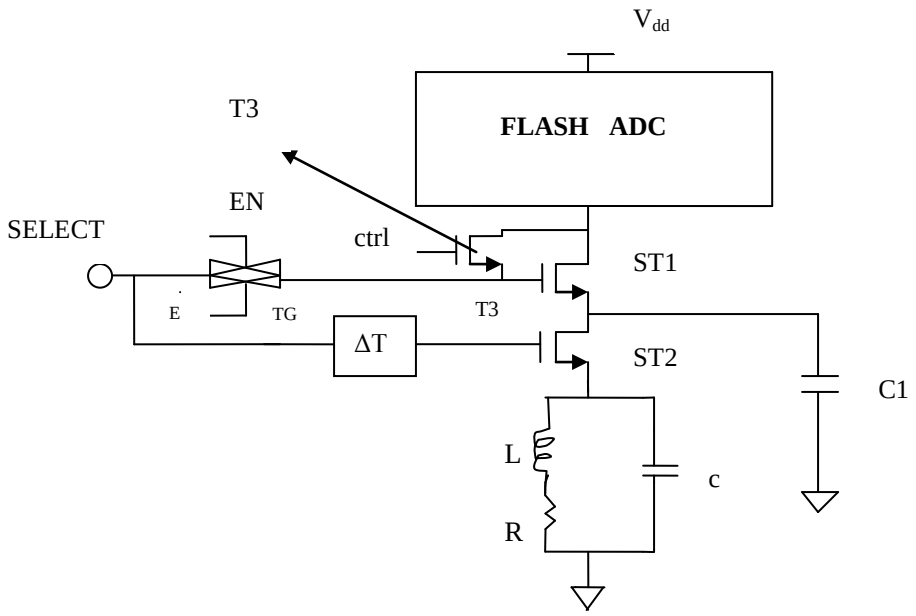


Figure 4. Flash ADC Design with Diode based Stacking Power Gating Technique

$$\text{Voltage across } C1 = V_{C1}(\text{active mode}) = V(R1_{ON} + R2_{ON}) \quad (1)$$

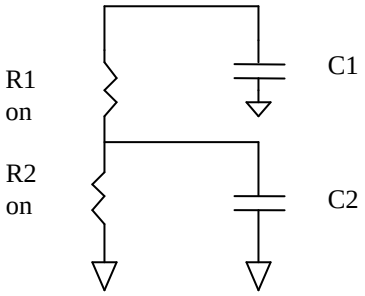
$$\text{Voltage across } C2 = V_{C2}(\text{active mode}) = V(R2_{ON}) = 0 \quad (2)$$

3.2. Standby Mode

Sleep transistor's ST1 & ST2 are OFF in standby mode therefore

$$\text{Voltage across } C1(\text{standby mode}) = V_1 \quad (3)$$

$$\text{Voltage across } C1(\text{standby mode}) = V_2 \quad (4)$$



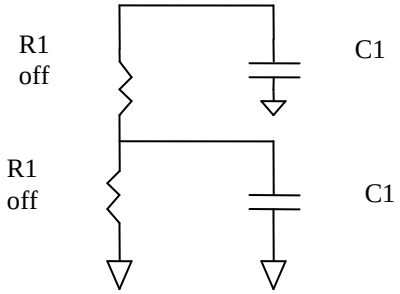


Figure 5 Figure 6

Figure 5. Equivalent Circuit of Sleep Transistor ST1 and ST2 in Active Mode
Figure 6. Equivalent Circuit of Sleep Transistors ST1 and ST2 in Standby Mode

Positive potential is generated at the intermediate nodes having different effects which are described below:

- Gate to source voltage (Vgs1) is applied at ST1 transistor became negative.
- Negative potential at body to source terminal (Vbs1) of control transistor T3 cause body effect.
- Negative potential at body to source terminal (Vds1) of sleep transistor ST1 decline, affecting in lower drain induced barrier lowering (DIBL).
- Drain to source potential (Vds2) of sleep transistor ST2 is lower as compared to control transistor T3, occur due to voltage drop across ST1. This mainly reduces the drain induced barrier lowering (DIBL).

3.3. Sleep to Active Mode

When the circuit is operated in sleep-to-active mode & vice-versa then ground bounce noise reduction is reported in the circuit. During the first stage, sleep transistor (ST1) behave as a diode by turning ON the control transistor (T3) that become forward biased stage and this control transistor is connected across drain and gate of transistor (ST1). By turning ON the control transistor, the reduction of the voltage fluctuation on the ground moreover reduction of the wakeup time occur, therefore initially transistors (ST1) turn ON and control transistor T3 must also turn ON but after some delay for reducing the ground bounce noise. During the second stage, the sleep transistor works as normal manner when the control transistor (T3) is OFF. In sleep to active mode, control transistor T3 is ON and sleep transistor ST2 is turned ON after some delay for reducing the ground bounce noise. Ground bounce noise is reduced effectively during this mode of operation.

4. Simulation and Performance Characteristics

4.1. Active Power Simulation

The power is dissipated by the circuit at the time of the operation is known as active power. Active power contains both dynamic and static power. We calculated the active power of the circuit at different voltages for the 45nm technology. Active power also calculated by equation [25].

$$P_{act} = P_{dyna} + P_{stat} \quad (5)$$

$$P_{act} = P_{swi} + P_{s-c} + P_{leak} \quad (6)$$

$$P_{act} = (\alpha_{0\to1} \times C_{load} \times V_{dd}^2 \times f_{clock}) + (I_{s-c} \times V_{dd}) + (I_{leak} + V_{dd}) \quad (7)$$

Where,Pact=active power,Pdyna=dynamic power,Pstat=static power,Pswi=switching powr,Ps-c=short circuit power,Pleak=leakage power,Cl = capacitance at load, fclock = frequency at clock, α = switching activity, Is-c = current when circuit is short, Ileak = leakage current, Vdd = supply voltage.

Table1. Active Power of Flash ADC

Different voltages(volts)	Active power(μW)
0.5	45.22
0.7	46.11
0.9	46.72
1.1	50.05

It clearly indicates that flash ADC with diode based stacking power gating scheme, active power is greatly reduced as compared to conventional design. Reduction of 16% active power achieves after using diode based stacking power gating technique.

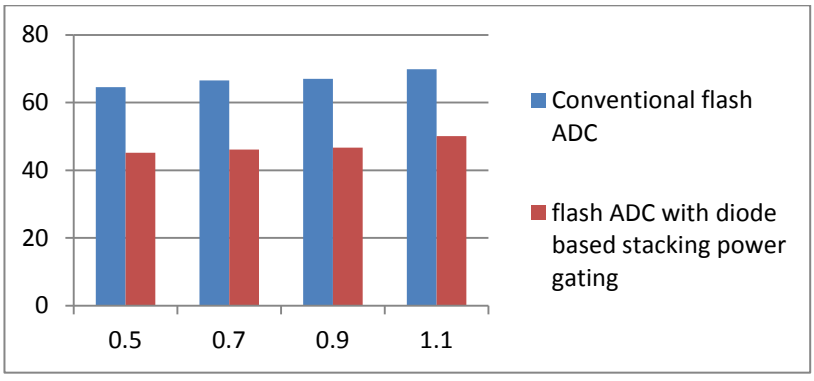


Figure 7. Active Power Dissipation of 3 Bit Flash ADC

4.2. Leakage Current Simulation

Leakage current of the flash ADC is estimated during the standby mode. To estimate the leakage current of the flash ADC, NMOS transistor is required to measure the leakage current that is connected at the pull down network below the whole circuit. Sleep transistor is OFF for this technique whenever leakage current calculation is analyzed. Leakage current is derived and calculated by the equation given below [26].

$$I_{leak} = I_{sub-thr} + I_{gat-ox} \quad (8)$$

Where, Isub-threshold = sub-threshold leakage current, Igat-ox = gate-oxide leakage current.

$$I_{sub-threshold} = K_A W e^{\frac{-V_{th}}{nV_\theta}} (1 - e^{\frac{-V}{V_\theta}}) \quad (9)$$

Where, KA and n are experimentally derived, W = gate width, Vth = threshold voltage, n = slope shape factor, VΘ = thermal voltage.

$$I_{gat-ox} = K_B W (\frac{V}{T_{ox}})^2 e^{\frac{-\alpha T_{ox}}{V}} \quad (10)$$

Where, KB and α are experimentally derived, Tox = oxide thickness

Table 2. Leakage Current Analysis at Different Voltages

Different voltages(volts)	Leakage current(nA)
0.5	113.40
0.7	164.37
0.9	202.48
1.1	287.93

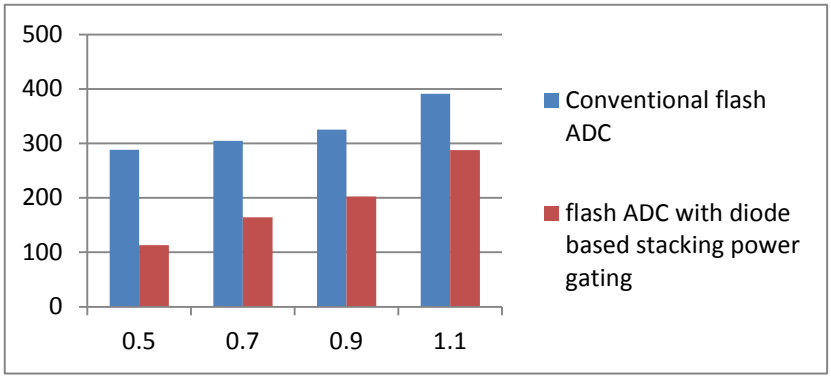


Figure 7.Leakage Current of 3 Bit Flash ADC

It clearly indicates that flash ADC with diode based stacking power gating scheme, active power is greatly reduced as compared to conventional design. Reduction of 82% leakage current is achieved after using diode based stacking power gating technique.

4.3. Leakage Power Simulation

The leakage power of the circuit is measured during the standby mode. It explained that how several percentage of power is wasted by the whole circuit during off state condition whenever there is no supply. Leakage power is the product of the leakage current and supply voltage. The basic equation of leakage power is realized by Equation. (12) [25]

$$P_{leak} = I_{leak} \times V_{dd} \quad (11)$$

Where, Ileak = leakage current, Vdd = supply voltage.

Table 3. Leakage Current Analysis at Different Voltages

Different voltages(volts)	Leakage power(nW)
0.5	56.7
0.7	115.05
0.9	182.23
1.1	316.723

It clearly indicates leakage power is reduced to 73% with diode based stacking power gating scheme.

4.4. Ground Bounce Noise Reduction

Ground bounce noise affects the performance of ADC by changing the output data into different code values. Some codes are missed during ground bounce which is generated in the flash ADC therefore device performance degrades. Ground bounce noise produced by the diode based stacking power gating scheme is characterized in this section. We used a well-characterized 40-pin Dual In-Line Package (DIP - 40) model in this paper to evaluate the ground bounce noise [26]. The model of DIP-40 is shown in figure. Ground bounce noise occurs when the circuit is going from sleep to active mode and vice-versa. The noise immunity of a circuit decreases as its supply voltage reduces.

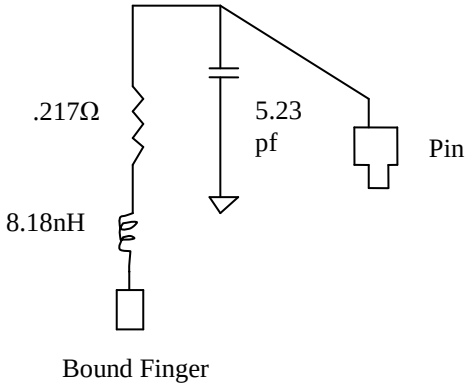


Figure 8. DIP-40 Package Pin Ground Bounce Noise Model

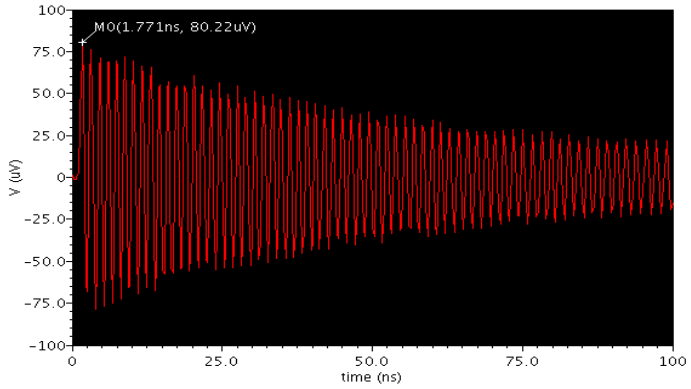


Figure 9. Showing Ground Bounce Nosie of Flash ADC

Ground bounce noise is reduced effectively in designed flash ADC with diode based power gating technique as compared to conventional design. Ground bounce noise is reduced up to 73 % with this technique.

Signal to noise ratio (SNR) [27] can be calculated with the help of peak amplitude of signal and noise. Ground bounce noise is shown in Figure 9 and SNR can be calculated by given equation.

$$\mathrm{SNR} = 20\log_{10}\left(\frac{\mathrm{A_{signal}}}{\mathrm{A_{noise}}}\right)\mathrm{dB} \qquad (12)$$

Where Asignal and Anoise is the peak amplitude of signal and noise.

Table 4. Performance Comparison of Conventional Flash ADC and Flash ADC with Diode based Stacking Power Gating Technique

Parameters	Conventional flash ADC	Flash ADC with diode based stacking power gating technique
SNHR	5.817 dB	160.4 dB
SFDR	5.967 dB	5.636 dB
SNR	56.36 dB	78.81 dB
ENOB	3.45-bit	0.152 –bit

Table 4 describes the diode based stacking power gating technique effect on the performance of conventional flash ADC. It clearly indicates that diode based power gating technique improve the performance of ADC that degrade due to the ground bounce noise effect.

5. Conclusion

In this paper low leakage “3” bit flash ADC is designed for signal processing and communication systems and design of flash ADC with the improved diode based stacking power gating technique describe for ground bounce noise analysis. A high performance diode based stacking power gating technique has been used to minimize the ground bounce noise and control the leakage power during the sleep to active mode transition. The ground bounce noise is restricted with the help of a delayed select signal associated by using a stacked sleep transistor. In diode based stacking power gating technique, the ground bounce noise is controlled by using a stacked sleep transistor with the help of a delayed select signal. The leakage power and leakage current are reduced by 79% and 82% with diode based stacking power gating technique in comparison to conventional flash ADC. Ground bounce noise is reduced by 75% with diode based stacking power gating technique in comparison to conventional flash ADC. Active power is reduced up-to 14% with diode based stacking power gating technique.

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References

[1] Y. L.Wong, M. H. Cohen and P. A. Abshire, “A 750-MHz 6-b adaptive floating-gate quantizer in 0.35-µm CMOS”, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 7, **(2009)** July, pp. 1301-1312.
[2] Z. Wang and M.-C. F. Chang, “A 1-V 1.25-GS/S 8-bit self-calibrated flash ADC in 90-nm digital CMOS”, IEEE Tran. Circuits Syst. II, Exp. Briefs, vol. 55, no. 7, **(2008)** July, pp. 668-672.
[3] Z. Wang and M.-C. F. Chang, “A 600-MSPS 8-bit CMOS ADC using distributed track-and-hold with complementary resistor/capacitor averaging”, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 11, **(2008)** December, pp. 3621-3627.
[4] A. Stojcevski, H. P. Le, A. Zayegh and J. Singh, “Flash ADC Architecture”, IEEE Electronic Letters Journal, **(2003)** February.
[5] G. Temes, “Micropower data converters: A tutorial”, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 6, **(2010)** June, pp. 405-410.
[6] T. Sundstrom and A. Alvandpour, “Utilizing process variations for reference generation in a flash ADC”, IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 5, **(2009)** May, pp. 364-368.
[7] S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim and U. Moon, “Stochastic flash analog-to-digital conversion”, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 11, **(2010)** November, pp. 2825-2833.
[8] C. Y. Chen, M. Le and K. Y. Kim, “A low power 6-bit flash ADC with reference voltage and common-mode calibration”, Symp. VLSI Circuits Dig., **(2008)** June, pp. 12-13.
[9] K. Uyttenhove and M. Steyaert, “A 1.8 V 6-bit 1.3 GHz flash ADC in 0.25 □m CMOS”, IEEE J. Solid-State Circuits, vol. 38, no. 7, **(2003)** July, pp. 1115-1122.
[10] M. R. Meher, C. C. Jong and C.-H. Chang, “A High Bit Rate Serial-Serial Multiplier with On-the-Fly Accumulation by Asynchronous Counters”, IEEE Trans. On Very Large Scale Integr. (VLSI) System 2011, vol. 19, no. 10, pp. 1733-1745.
[11] D. Bailey, E. Soenen, P. Gupta, P. Villarrubia and D. Sang, “Challenges at 45 nm and beyond”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), **(2008)**, pp. 11-18.
[12] H. Singh, K. Agarwal, D. Sylvester and K. J. Nowka, “Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 15, no. 11, **(2007)**, pp. 1215-1224.
[13] S. Kim, C. Jun Choi, D.-K. Jeong, S. V. Kosonocky and S. Bae Park, “Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures”, IEEE Transactions on Electron Devices, vol. 55, no. 1, **(2008)**, pp. 197-205.

[14] J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 11, **(2006)**, pp. 1250-1263.
[15] H. Jiao and V. Kursun, "Noise-Aware Data Preserving Sequential MTCMOS Circuits with Dynamic Forward Body Bias", Journal of Circuits, Systems and Computers, vol. 20, no. 1, **(2011)**, pp. 125-145.
[16] B. Gupta and S. Nakhate, "Transistor Gating: A Technique for Leakage Power Reduction in CMOS Circuits", International Journal of Emerging Technology and Advanced Engineering, vol. 2, no. 4, **(2012)**, pp. 321-326.
[17] Design, implementation and analysis of flash adcarchitecture with differential amplifier as comparator using custom design approachchannakka lakkannavar, 2shrikanth k. shirakol, 3kalmeshwar n. hosur.
[18] D. J. Banks, P. Degenaar and C. Toumazou, "Distributed Current-Mode Image Processing Filters", H. Traff, "Novel approach to high speed CMOS current comparators", Electronics Letters, vol. 28, no. 3, **(1992)**, pp. 310-312.
[19] X. Tang and K.-P. Pun, "High-performance CMOS current comparator", Electronics Letters, vol. 45, no. 20, **(2009)**, pp. 1007-1009.
[20] A. T. K. Tang and C. Toumazou, "High performance CMOS current comparator", Electronics Letters, vol. 30, no. 1, **(1994)**, pp. 5-6.
[21] L. Ravezzi, D. Stoppa and G.-F Dalla Betta, "Simple High-speed CMOS current comparator", Electronics Letters, vol. 33, no. 22, **(1997)**, pp. 181830.
[22] A. Dingwall, "Monolithic Expandable 6 Bit 20 MHz CMOS/SOS AID Converter", Solid-State Circuits, IEEE Journal of, vol. 14, no. 926-932, **(1979)**.
[23] D. Subedi and E. John, "Stand-by Leakage Power Reduction in Nanoscale Static CMOS VLSI Multiplier Circuits Using Self Adjustable Voltage Level Circuit", International Journal of VLSI Design and Communication Systems (VLSICS), vol. 3, no. 5, **(2012)**, pp. 1-11.
[24] N. H. E. Weste, D. Harris and A. Banerjee, "CMOS VLSI Design: A Circuit and System Perspective", Pearson Education, Third Edition, **(2011)**.
[25] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicron CMOS Circuits", Proceedings of the IEEE 2003, vol. 91, no. 2, pp. 305-327.
[26] H. Jiao and V. Kursun, "Ground-Bouncing-Noise-Aware Combinational MTCMOS Circuits", IEEE Transactions on Circuits and Systems, vol. 57, no. 8, **(2010)**, pp. 2053-2065.
[27] S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath and P. Wilkins, "A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS pipeline ADC", IEEE ISSCC Dig. Tech. Papers, **(2009)** February, pp. 86-87.

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