Adaptive Method for Minimization of Power Consumption in Sequential Circuits Through DVS and Error Prediction

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Abstract

This paper presents Adaptive methodology to compensate the On Chip Variations (OCV), aging effect and manufacturing uncertainties in sub threshold circuits. "Canary flip-flop (FF)," is used to predict the timing violations. A FSM, 4-bit Counter, in CMOS 90nm technology whose performance is controlled by automatically changing voltage levels (DVS) as per the timing error prediction. In addition, the voltage supply is further scaled down if no timing error is predicted within certain time period to save more power at different PVT conditions. Back end simulation results shows, the design under observation with this technique can compensate process, supply voltage and temperature instability with an efficient power savings of nearly 40% with respect to the conventional worst case design with timing margins approach. Here we also demonstrate how to define the delay of delay chain during the design phase itself.

Keywords: *OCV, Sub-threshold circuits, DVS, DVFS, Canary Technique, Timing Violations, Adaptive compensation and delay chain*

1. Introduction

The most critical concern in sub threshold circuits is to achieve high level of performance with very tight power constraints [1, 2]. This is evident in the development of mobile phones: in last one decade talk-time per gram of battery has improved by 60x. Challenges that prevent sub-threshold circuits from being widely used are their performances dependency on different Process Voltage and Temperature (PVT) conditions. That is why the classical guard band methodology for "worst-case" is no more efficient, so some adaptive performance control techniques are required. Initially, the most critical paths of the circuits were replicated to track the correct functionality. Reference [3] represents an application of adaptive performance control with replica circuit but, original critical path circuit and its replica part can't be identical from manufacturing point of view. To address these issues, different adaptive techniques [4-6] were proposed.

Initially error detection based techniques [4-6] were adopted and then improved [7] by the time and named as Razor technique. As error detection techniques are dependent on re-execution [8, 9] loss of real time execution. In case of pipe line circuits these techniques were not at all preferred because in case of error is caught whole pipeline is supposed to be flushed and reassumed from the point of failure. Razor and modified razor technique can be well understood by Figure 1and 2 respectively.

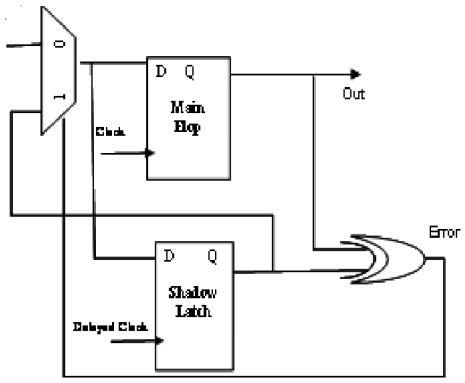

Figure 1. Razor Flip Flop

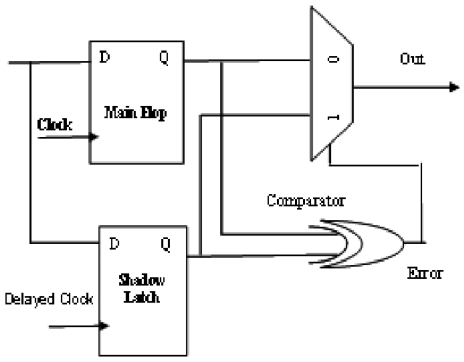

Figure 2. Modified Razor Flip Flop

To compete with the limitation of the timing error detection based techniques, timing error prediction based techniques were required, so that the corrective measures can be taken before its occurrence. This technique was later proposed and named as Canary technique [10, 11]. As in case of canary technique occurrence of error is avoided so there, no corrective action is required [12, 13]. This way limitation of additional circuit and time to complete the re-execution process was avoided. Canary technique can be understood by Figure 3. Later part of the paper, presents implementation of Canary technique along with DVS technique [14] applied on a 4-bit sequential counter circuit (Finite State Machine (FSM)). This is an adaptive technique which can tune the subsystem efficiently to act as robust, reliable and power efficient.

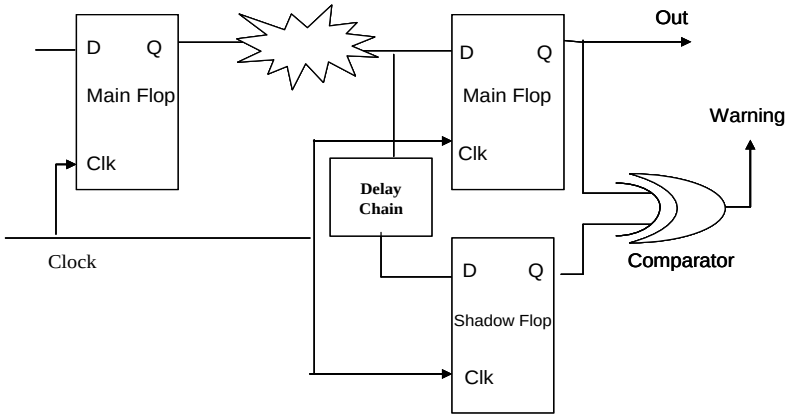

Figure 3. Canary Flip Flop

2. Auto-Adaptive Speed and Power Control

A FSM, 4-bit synchronous counter circuit is adopted to be analyzed. Complete subsystem is explained in below subsections:

2.1. Overview

Figure 4 shows the schematic overview of Auto-adaptive speed and power [15, 16] control logic with Canary Flip-Flop consists of a shadow Flip-Flop whose out is

compared with the main Flip-Flop of the counter logic. Input of the shadow Flip-Flop tapped from the input of the main Flip-Flop through a delay chain. The comparator output is taken to a "monitor and speed control" logic, where it is monitored and decided whether the logic is having enough margin to produce correct output or not.

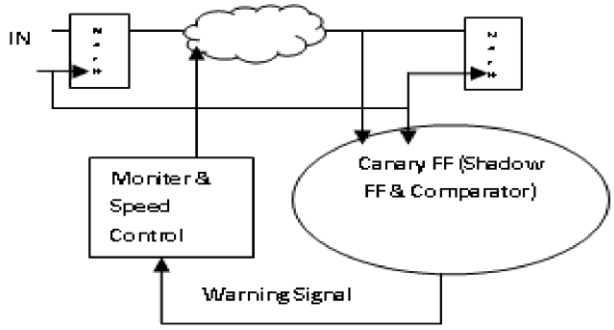

Figure 4. Schematic Overview of Subsystem

Monitor and speed control logic is a FSM which works on the basis of some inputs like warning, clock and reset etc.

If, Warning = '1' → Comparator output showing mismatch, circuit need to be Speed-up.
= '0' → If this no mismatch occurs for more than certain time period means, circuit has Enough timing margin to be speed down to reduce power consumption.

2.2. Block Level Architecture

As shown in Figure 5 each Flip-Flop of main DUT (4-bit sync counter) is tracked with its individual shadow Flip-Flop (Canary Flip-Flop). Each Canary Flip-Flop is a combination of comparator and a configurable delay chain unit. Each comparator output is traced in monitor and speed control unit to generate the warning signal in case of any timing violation. Monitor and speed control, supply voltage selection and timer units always work at highest available voltage to get always correct functionality from these units.

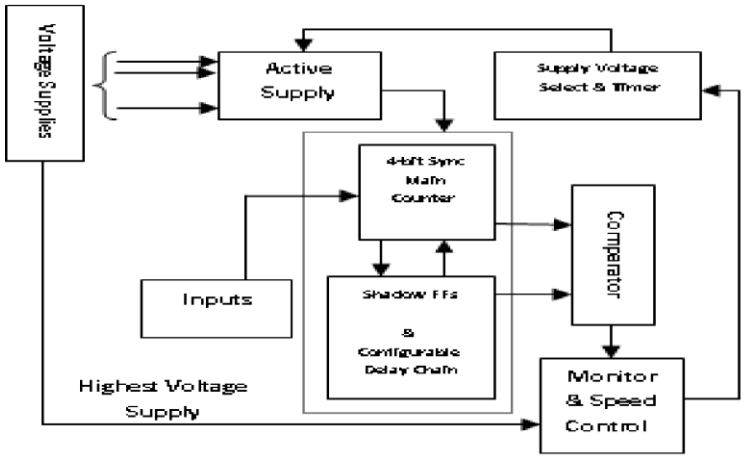

Figure 5. Block Diagram of Auto Controlled 4-bit Sync Counter with Canary

3. Implementation

The implementation is carried in the following steps.

3.1 Flow, Tools and Technology

First of all schematic of the counter is drawn with different required instances of HVT cells in cmos90 nm technology. Designed the monitor and speed control unit in RTL and its SPICE netlist is generated. Now both counter with canary Flip-Flop schematic's SPICE netlist and monitor and speed control unit SPICE netlist are integrated at top level and the integrated sub-system is taken into ELDO for simulations at different supply voltage and temperatures. Simulation results are analyzed with Ezwave which are further discussed in Section 5.

3.2 Overview

The designed test circuit architecture consists of DUT and monitor and speed control, timers, voltage selection unit and some power switches as shown in Figure 5. A 4-bit synchronous counter is adopted as a circuit whose performance is analyzed at different PVT conditions in 90nm CMOS technology with and without Canary Flip-Flop implementation. All the observations are done at three different voltage supplies: 2.7V, 3.0V and 3.3V and different temperature -40^{o}C, 27^{o}C and 150^{o}C and their different combinations.

3.3. Canary/Shadow Flip-Flop Implementation

Outputs of main counter Flip-flops are Q [0], Q[1], Q[2] and Q[3] where Q[0] is LSB and Q[3] is MSB. Each output bit of main Flip-Flop is compared with respective shadow Flip-Flop output as shown in Figure 6 to trace the timing error at any bit if occurs.

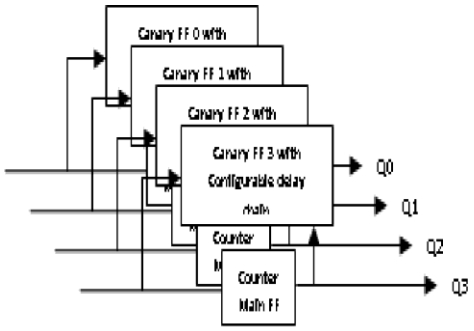

Figure 6. Bit by bit Canary Implementation

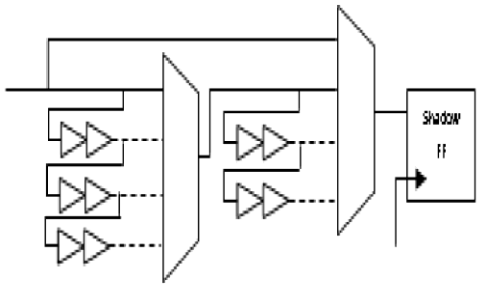

Figure 7. Configurable Delay Chain Implementation

3.4. Delay Chain Implementation

The implemented Canary Flip-Flop consists of a delay chain, designed in a way that its delay is configurable to different values as per the DVS adaptive supply voltage state respectively. Each Canary Flip-Flop and its configurable delay chain can be very well understood from Figure 7. As it is shown above each Canary Flip-Flop has its own configurable delay chain. The delay of the individual delay chain can also selected adaptively w.r.t the selected voltage level.

3.5 Adaptive Technique Implementation

Whenever there is any mismatch between the main Flip-Flop and shadow Flip-Flop warning signal is generated and sent to the monitor and speed control unit where the current state of Finite State Machine selects which voltage supply is need to be connected respectively. If there is no warning signal generated for a certain defined time period, a slow down signal is generated. This slow down signal helps to scale down the applicable voltage of the design, to reduce the power consumption during run or standby modes. This whole implementation can be understood in Figure 5. Blocks like speed and monitor control, voltage selection, timers and supply selection switches always supplied with highest available voltage supply to get always an expected and correct behavior.

Figure 8 shows the condition of no warning signal generation in-case there is no timing error as the counter and shadow Flip-Flops are giving expected values at each and every clock cycle.

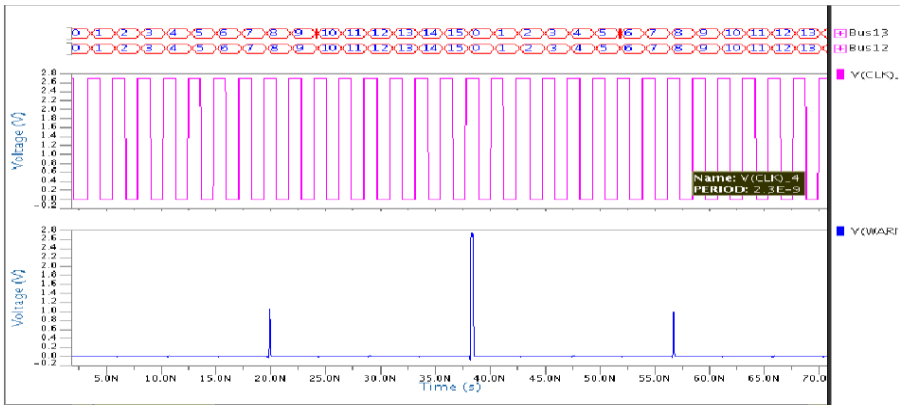

Figure 8. Normal Functionality of the Design without Error

4. Measurements and Results

Different measurements and results are collected as shared below in detail:

4.1. Delay chain Calibration

Canary Flip-Flop delay chain can be configured individually with respect to the selected supply voltage of the DUT. The configured delay of the buffer is measured by following procedure:

1. Some input is given to the circuit to toggle the counter Flip-Flops.

2. Applied clock frequency is swept with a starting value where there is no timing error till the error occurred in shadow Flip-Flop and warning signal is generated. Assume that clock Period is P_s.

3. Applied frequency is swept further till functional/main Flip-Flop and shadow Flip-Flop as well starts giving timing error. Assume that clock period is P_f.

Difference between P_s and P_f determine the required delay of buffer chain and by averaging out, individual buffer delay is calculated. This whole exercise is repeated at different available voltage levels and at temperature combinations. The outcome is

presented below with the help of graph in Figure 9. Different voltage level are expressed along X-axis and delay values are expressed along Y-axis. Observations are done at different temperatures of -40C, 27C and 150C which helped to adopt the delay value in accordance to the supply voltage.

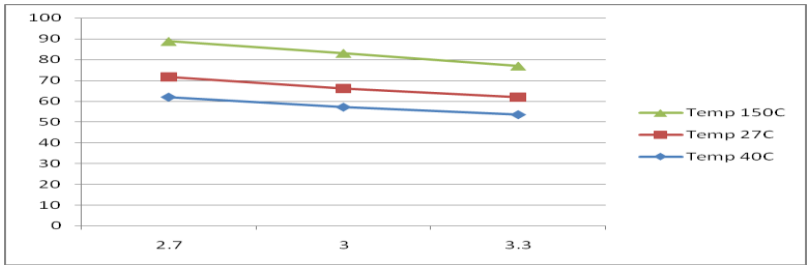

Figure 9. Delay Values at Different Supply and Temperature Values

4.2 Adaptive Compensation of Voltage with DVS

Figure 10 represents the power dissipation of the whole subsystem at 3.3V, 3.0V and 2.7V for different temperature values respectively. Here it can be understood that more the supply voltage is higher the power consumption of the system. There are very rare chances that system works at worst case conditions, from this can be understood that optimizing the circuit for worst case is not always utilized for same and power is properly utilized. By adaptive compensation technique the higer voltage is only applied when and only when reqired.

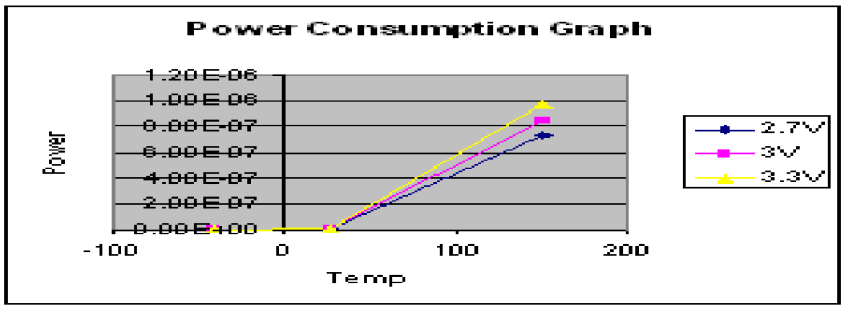

Figure 10. Power Consumption at Different Power Supply and Temperature

4.3 Ramping Up the Active Power Supply

As from the graphs it is clear that the power dissipation directly depends on the supply voltage. In adaptive speed controller, canary Flip-Flop might face timing error but the main Flip-Flop captures the correct value so the main circuit behaves correctly. This is because timing constraints of canary Flip-Flop are tighter then the main Flip-Flops. As shown in Figure 11 in case of timing error at canary Flip-Flop warning signal is asserted. Adaptive controller ramps up the power supply to the next higher level to maintain the correct functionally. As evident from Figure 12 when there is change of state of the monitor and speed control unit due to some timing error, it changes the active power supply accordingly.

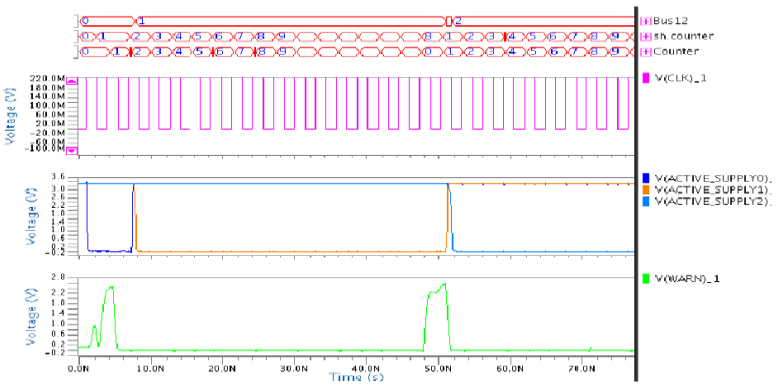

Figure 11. Warning Signal Generation with Timing Error

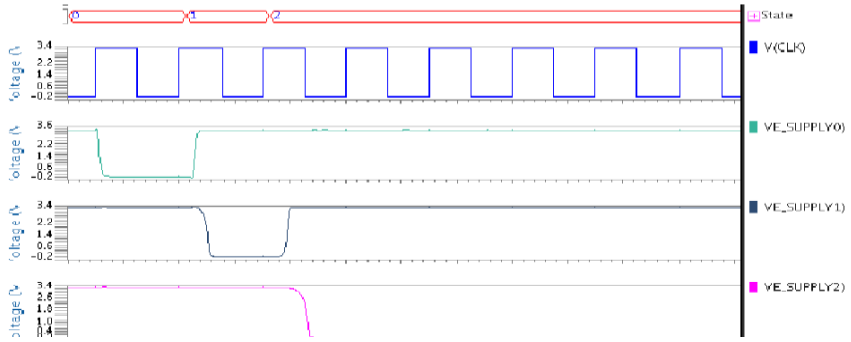

Figure 12. Adaptively Changing the Active Power Supply

4.4 Ramping Down the Active Power

In case of no warning signal is generated for a certain period (in our example used a counter counting till 4096 cycles) the controller steps down the power supply and waits again for some more time and if there is no timing error again then further, steps down the power supply voltage. Finally in case of no timing error maintains the lowest voltage level shown in Figure 13 is adopted to minimize the power dissipation.

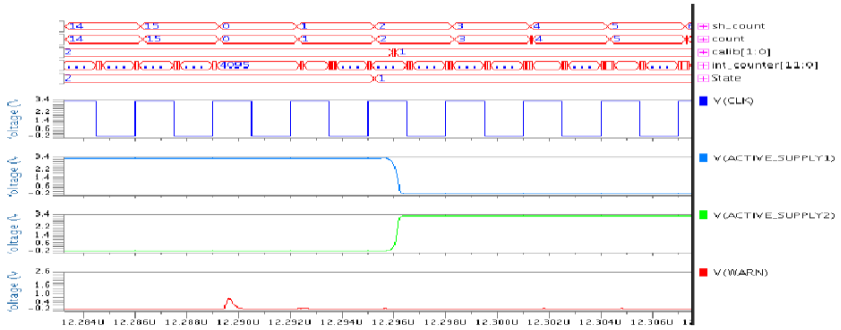

Figure 13. Ramping Down of the Active Power Supply

5. Conclusion

This paper presents the self-adaptive technique for compensation using canary Flip-Flop and DVS. A FSM of 4-bit synchronous counter performance is controlled by changing the

voltage supply adaptively. The simulations shows that the counter works at the maximum possible frequency and chooses itself its required highest available supply voltage. Whole sub-system is designed in 90nm CMOS technology and analysis results shows that with adaptive compensation technique power dissipation is reduced by nearly 38% compared to the worst case considerations of timing margins. Here it is also discussed how to calibrate the delay chains which is important to attain higher reliability and performance of the circuit.

6. Future Scope

As for as DVS and DVFS techniques are concern there is no automated solution or support available from Electronics Design Automation (EDA) industry which can make their implementation to be fast and hassle free. Some more work is expected on the requirement of high level characterization for delay chain cells and timing margins, required in Canary technique which is capable to predict and correct the timing error at the same time.

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