Simulation and Analysis of Gate Engineered Triple Metal Double Gate (TM-DG) MOSFET for Diminished Short Channel Effects

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Abstract

A triple metal double gate (TM-DG) MOSFET with high-k dielectrics has been proposed to overcome the short channel effects. We are using top and bottom metal gates with different work functions to screen the effect of drain (DIBL effect). It has been found that this is effective in reducing the short channel effects. The metal gates have been used to remove the poly silicon depletion of conventional double gate (DG) MOSFET due to aggressive scaling to sub 100 nm regimes. It has been observed that use of metal gate with different workfunctions along with high-k dielectric improves the carrier transport in the channel.

Keywords: *DG MOSFETs, high-K dielectrics, subthreshold swing*

1. Introduction

As conventional MOSFETs channel lengths are scaled down below 100 nm for improved performance and packing density, the gate oxide thickness is also scaled below 3 nm. Due to this aggressive scaling short channel effects (SCEs) like threshold voltage roll-off, gate leakage current, drain induced barrier lowering (DIBL), hot electron effects (HCEs) play a major role in determining the performance of scaled devices. These effects need to be minimized for proper operation of the MOSFETs. As the device size is scaled down the electric flux from the drain penetrates into the channel, thereby controlling the channel charge (electron/hole) and hence reducing the gate control over the channel charge. This reduces the source/channel barrier and hence increasing the OFF state leakage current, threshold voltage roll-off and subthreshold slope. For the low-power and high-speed operations, subthreshold swing (SS) for a steep transition from OFF state to ON state and the DIBL should be as smaller as possible. The smaller values of SS and DIBL also improve the ON/OFF current (I_{ON}/I_{OFF}) ratio.

The double gate (DG) MOSFETs are electro-statically superior to a single gate (SG) MOSFET and allows for additional gate length scaling [1]. Such scaled devices would necessitate very thin Si films ($t_{Si} < 10nm$) such that t_{Si} would influence the inversion-carrier energy quantization and mobility [2]. For symmetrical or nearly symmetrical-gate DGMOSFETs, volume inversion [3] can be obtained for thin t_{Si} that can potentially benefit the mobility [2]. The volume inversion "weakens" for increasing t_{Si} and/or ε_{Si}.

To enhance the immunity against the SCEs and therefore improving the device reliability in high performance circuit applications, a device using triple material (**TM**) and **DG**-MOSFET in sub-100 nm regime, was proposed by Orouji [4]. In TM-DG MOSFETs, the gate

electrode of the device consists of three laterally contacting materials with different workfunctions. Material workfunctions are selected in such a way that workfunction of the material near the source is highest and that near the drain is the lowest for n-channel MOSFETs (the opposite for p-channel). The high workfunction near the source leads to more rapid acceleration of carriers in the channel and the low workfunction near the drain leads to reduction of electric field peak at the drain side reducing HCEs. However, continual gate oxide scaling will require high-k gate dielectric; since the gate oxide leakage in SiO_2 is increasing with reducing physical thickness of gate oxide (SiO_2) and it will eventually run out of atoms for further scaling.

"High-k" stands for high dielectric constant, a measure of how much charge a material can hold. Different materials similarly have different abilities to hold charge. The higher "K" increases the transistor capacitance so that the transistor can switch properly between "ON" and "OFF" states, with very low current when OFF yet very high current when ON. Because high-k gate dielectrics can be several times thicker, they reduce gate leakage by over 100 times. As a result, these devices run cooler. Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without the increasing leakage effects.

$$C = \frac{K\varepsilon_0 A}{t_{ox}}$$

where A is capacitance area, K is the relative dielectric constant of the material, t_{ox} is the dielectric thickness and ε_0 is the permittivity of free space. This means higher K gives higher capacitance value.

2. TM-DG MOSFET Structure

Figure 1 shows the cross-sectional view of the triple metal double gate (TM-DG) MOSFET with high-K gate oxide. This structure is implemented using Sentaurus structure Editor (SentaurusSE). The device has been simulated using 2D device simulator Sentaurus Device. The Poisson's with density gradient mobility models have been solved for the TMDG MOSFET. The Density Gradient Quantization Model which can be applied to MOSFETs, quantum wells and SOI structures, and gives a reasonable description of terminal characteristics and charge distribution inside a device has been used in our simulations. Compared to the other quantization models, it can describe 2D and 3D quantization effects.

The details of device parameters used in the structure are shown in Fig. 1 and their symbols are given in Table 1. The entire device parameters have been taken to the reference values as shown in Table 1, unless specified otherwise.

We used a light channel doping concentration (1×10^{16} cm^{-3}) to avoid degradation of carrier mobility and threshold (V_t) variations [5,6]. We have also taken a graded doping profile between Source/Drain and channel of width 5 nm and doping 1×10^{17} cm^{-3} to avoid abrupt junction. The lengths of each gate materials (M1, M2 and M3) are 20 nm, with the workfunctions of the workfunctions of $\phi_{M1} = 4.8eV$ (Gold), $\phi_{M2} = 4.6eV$ (Tungsten) and $\phi_{M3} = 4.4eV$ (Titanium).

Surface phonon scattering in the high-k dielectric being the primary cause of channel electron mobility degradation, we use both SiO_2 and high-k dielectric (HfO_2) in the gate oxide. To avoid surface scattering due to the use of high-k dielectric as gate oxide; SiO_2 is used near the Silicon side (channel) with SiO_2 thickness (t_{SiO2}) =1 nm and high-k dielectric HfO_2 thickness (t_{HfO2}) = 4 nm.

Table 1. Device Dimensions and Dopings

Attributes	Value
Metal 1 length (Lgm1)	20 nm
Metal 2 length (Lgm2)	20 nm
Metal 3 length (Lgm3)	20 nm
Channel Doping (N_A)	$1.0x10^{+16}$ cm^{-3}
Source Doping (N_D)	$1.0x10^{+20}$ cm^{-3}
Drain Doping (N_D)	$1.0x10^{+20}cm^{-3}$

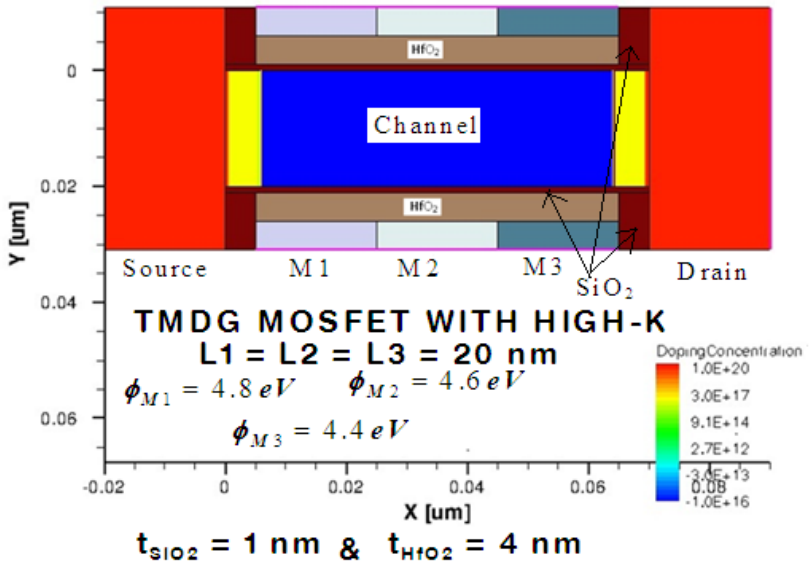

Figure 1. The TM-DG MOSFET with high-K

3. Results and Discussion

This section presents the performance analysis of TM-DG MOSFET with and without high-K (HfO_2) dielectric. Table 2 compares electrical characteristics of TMDG MOSFETs with various channel thickness. The values of V_{GS} and V_{DS} are 2.0 V. The electrical characteristics extracted are I_{ON}, I_{OFF}, g_m and V_{ggm} (gate voltage at which g_m is maxima). Table 2 shows that the structure with 5 nm channel thickness (t_{Si}) and high-k dielectric gives the lowest OFF state current (leakage current) with a minimal ON current reduction. In the rest of the paper only three channel thicknesses (5 nm, 10 nm and 20 nm) have been considered for comparison of various parameters for verifying that the devices with high-k are capable of reducing the SCEs and HCEs.

Figure 2 & 3 show the transfer characteristics of the TMDG MOSFETs with and without high-k with channel thickness of 5 nm and 20 nm respectively. It can be seen in the above transfer characteristics that the structures with high-k are having higher threshold voltage than their counterparts (without high-k). This is an indication of reduced OFF state current. In the strong inversion region, we can observe from the Fig. 2 and Fig. 3 that the ON state current is also improved for the structures with high-k.

Table 2. Electrical characteristics for different channel thickness. V_{GS} and V_{DS} = 2.0 V

MODEL	t_{Si} (nm)	I_{ON} (mA)	I_{OFF} (nA)*	g_m ($x10^{-3}$)	V_{ggm}
Without high-k	20	2.3	$6.191x10^{+3}$	1.489	1.997
Without high-k	5	1.7	$4.201x10^{+1}$	1.127	0.983
With high-k	20	.2.8	$1.393x10^{+1}$	1.930	0.992
With high-k	10	2.6	$2.582x10^{-1}$	1.778	1.996
With high-k	5	2.2	$1.626x10^{-2}$	1.601	0.625

* the OFF state current has been extracted for the value of V_{GS}=0 V

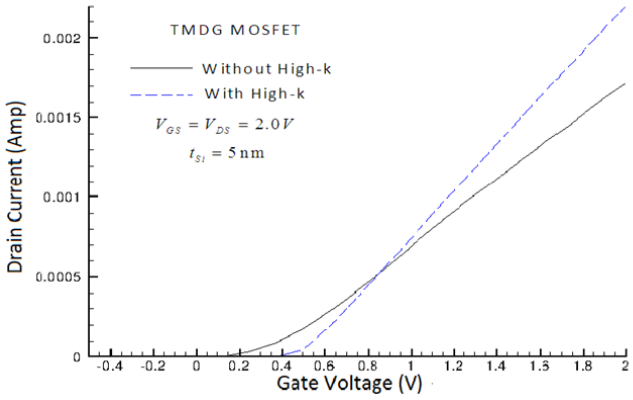

Figure 2. Drain current (I_D) vs. Gate voltage (V_{GS}) of TMDG MOSFETs with and without high-k for the Silicon film thickness of t_{Si}=5 nm for V_{DS}=V_{GS}=2.0 V

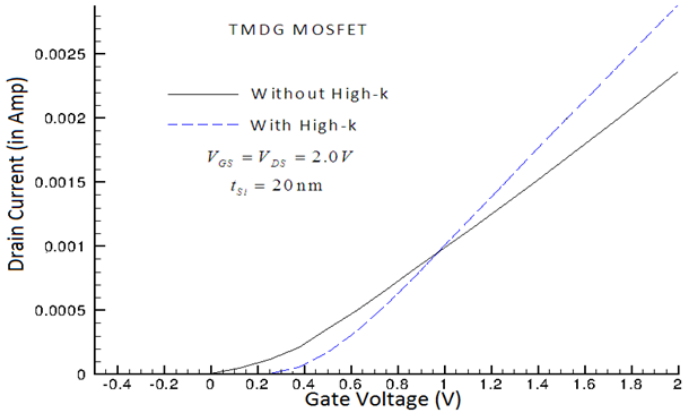

Figure 3. Drain current (I_D) vs. Gate voltage (V_{GS}) of TMDG MOSFETs with and without high-k dielectric for the Silicon film thickness of t_{Si}=20 nm and V_{DS}=V_{GS}=2.0 V

Table 3. Subthreshold swing (SS) of the structure for different channel thickness and for V_{DS}=V_{GS}=1.0 V

TMDG MOSFET	t_{Si} (nm)	SS
Without high-K	5	110.861
With high-K	20	96.680
With high-K	10	87.680
With high-K	**5**	**69.018**

Table 3 shows that the structure with 5 nm channel thickness with high-k gives the lowest subthreshold swing (SS) than other structures. It can also be observed that the SS is smaller even when we have a channel thickness of 20 nm with high-k than the device having a channel thickness of 5 nm without high-k. This verifies the fact that the use of high-k is able to reduce the short channel effects (SCEs).

Figure 4 shows the surface electric field along the channel for TMDG MOSFETs with and without high-k and single metal double gate (SMDG) MOSFET without high-K dielectric having the channel thickness of 10 nm. It is observed that the electric field at the drain side of TMDG MOSFET with high-k dielectric has higher electric field than the TMDG MOSFET without high-k dielectric but in SMDG MOSFET without high–K dielectric; electric field is higher than TMDG MOSFETs. It means that the hot electron effect is more pronounced in the case SMDG MOSFET without high-k dielectrics. Therefore, the use of high-k is capable of reducing the hot electron effects. Apart from this the electric field at the source end has also increased which causes more rapid acceleration of carriers in the channel showing increase in the electron injection velocity from the source into the channel. So the device without high-k is slower than the device with high-k.

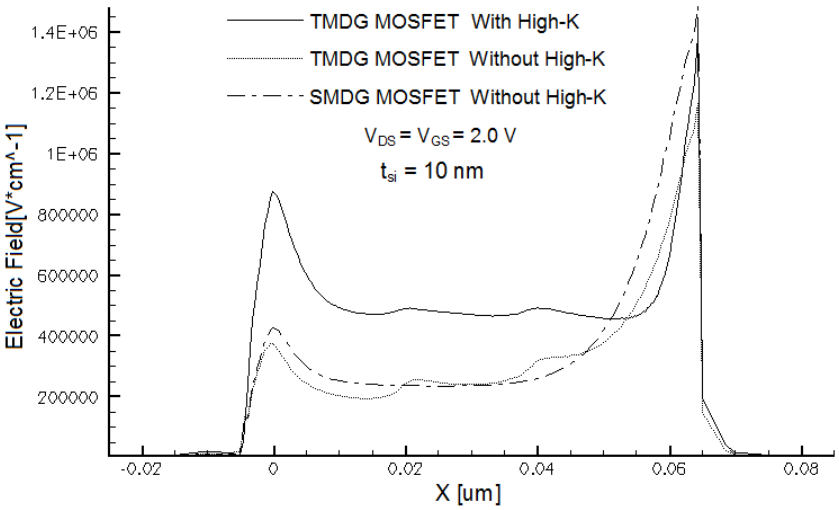

Figure 4. Surface Electric Field of TMDG MOSFETs with and without high-K dielectric and SMDG MOSFET without high-K dielectric (i.e. at y = t_{si} or 0) for the Silicon film thickness of t_{Si}=10 nm and V_{DS}= V_{GS}= 2.0 V

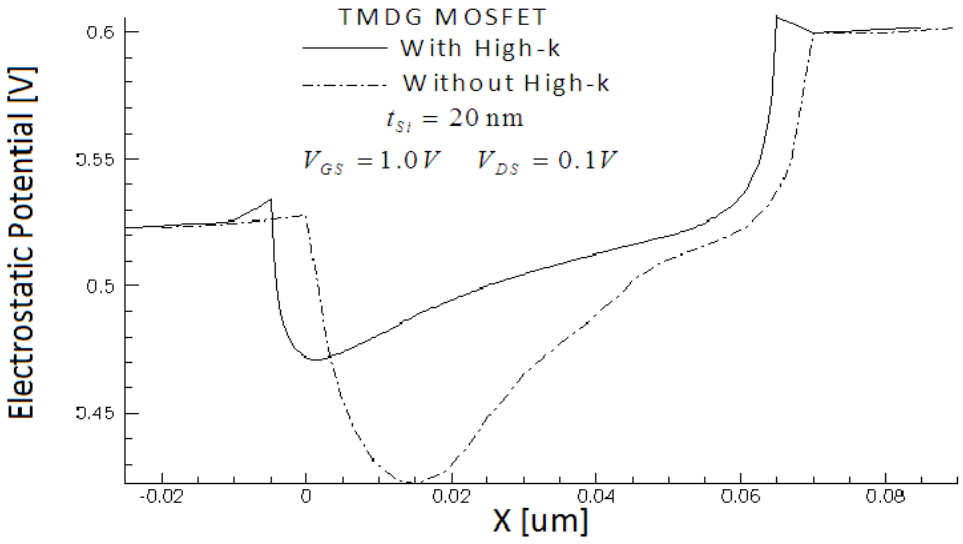

Figure 5. Electrostatic Potential of TMDG MOSFETs with and without high-K dielectric at the center of the channel ($y=T_{si}/2$) for the Silicon film thickness of t_{Si}=20 nm and V_{DS}=0.1V V_{GS}=1.0 V

In Fig. 5 the electrostatic potential in the middle of the channel of TMDG MOSFETs with/without high-k and channel thickness of 20 nm is shown. It can be seen in the figure that the electrostatic potential at the source end is very high for the device with high-k as compared to the device without high-k. It means that the injection of carrier from the source is at higher velocity and hence does not degrade the speed of operation of the device.

In Fig. 6 the electric field in the middle of the channel of TMDG MOSFETs with and without high-k and SMDG MOSFET without high-K dielectric, having the channel thickness of 10 nm are shown. It can be observed that the electric field near the drain end has decreased for the device TMDG MOSFET with and without high-k as compared to the device SMDG MOSFET without high-k, decreasing the hot electron effects. Though electric field in drain side of the TMDG MOSFET with high-k is slightly more causing hot electron effect but in source side acceleration of carrier to the channel is much higher than without high-k thus in overall TMDG MOSFET with high-k is improved one.

In Fig. 7 the electron density in the middle of the channel for TMDG MOSFETs with and without high-k is plotted. It can be observed that the electron density at the source end has improved for the device with high-k. This is due to the volume inversion taking place in the middle of the channel. The volume inversion in the channel improves the ON state drain current. So, the use of high-k increases the I_{ON}/I_{OFF} ratio.

In Fig. 8 the transconductance of TMDG with and without high-k for various channel lengths have been plotted. It is observed that the use of high-k significantly increases the transconductance for all the cases. From Fig. 9 it is observed that the I_{OFF} current for the device with high-k has reduced by approximately 10^4 times to that of without high-k. This offers a very high I_{ON}/I_{OFF} ratio.

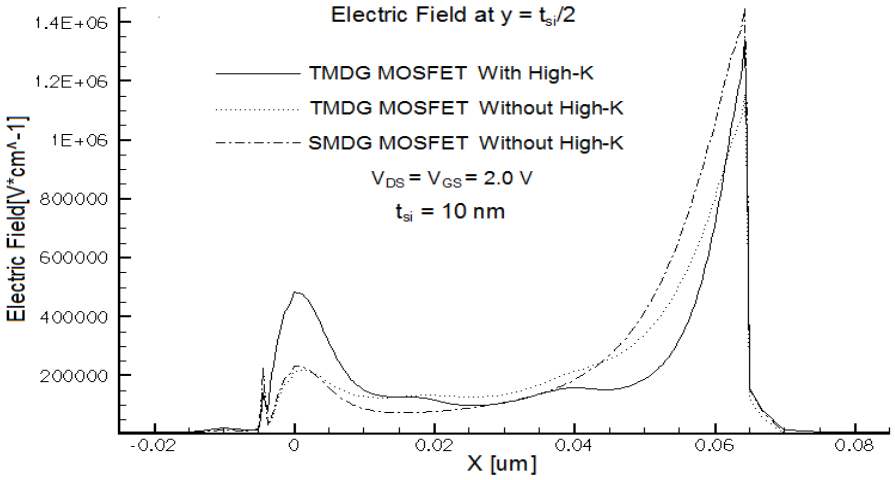

Figure 6. Electric Field of TMDG MOSFETs with and without high-K dielectric and SMDG MOSFET without high-K dielectric at y=T_{si}/2 for the Silicon film thickness of t_{Si}= 10 nm and V_{DS}= V_{GS}= 2.0 V

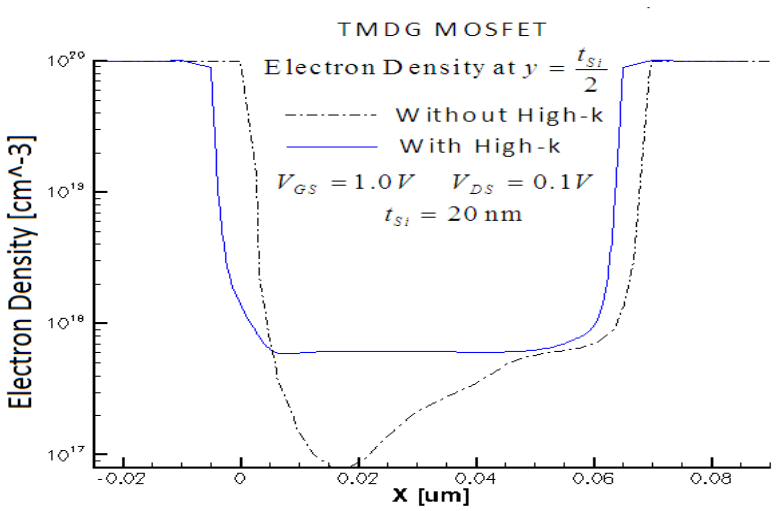

Figure 7. Electron density of TMDG MOSFETs with and without high-K dielectric at y=T_{si}/2 for the Silicon film thickness of t_{Si}=20 nm and V_{DS}=0.1V ,V_{GS}=1.0 V

Figure 10 shows the subthreshold swing for both TMDG MOSFETs with and without high-k for different channel lengths. It is observed that the use of high-k significantly reduces the subthreshold swing for the channel lengths in sub 100 nm regime. It is due to the use of metal gate materials with different workfunctions. Due to workfunction difference of gate metals, the main channel is screened of the variations in the drain voltage.

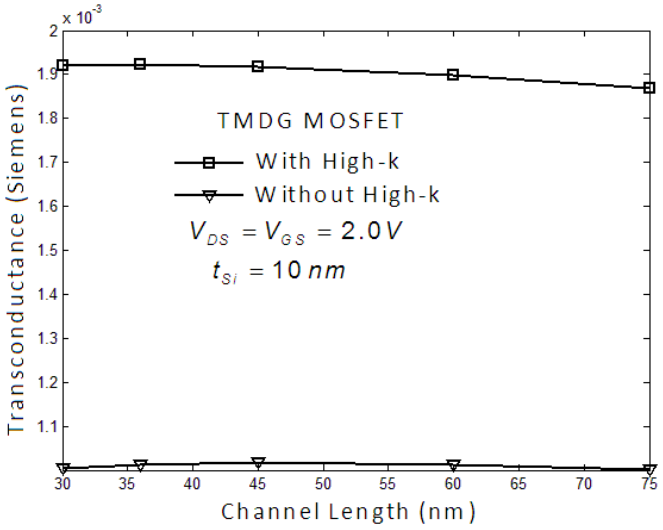

Figure 8. Transconductance vs channel length of TMDG MOSFETs with and without high-K dielectric for the Silicon film thickness of t_{Si}=10 nm and for V_{DS}=V_{GS}=2.0 V

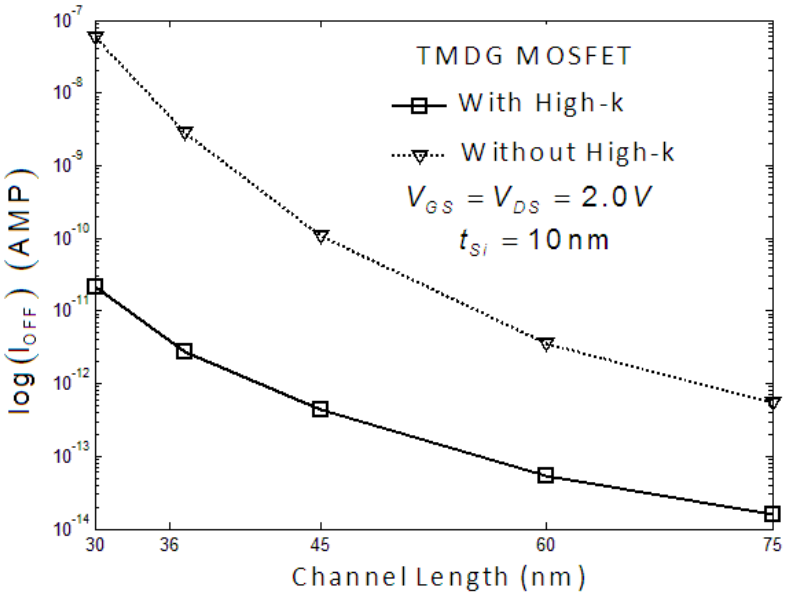

Figure 9. Log(I_{OFF}) vs channel length of TMDG MOSFETs with and without high-K dielectric for the Silicon film thickness of t_{Si}=10 nm and V_{DS}=V_{GS}=2.0 V

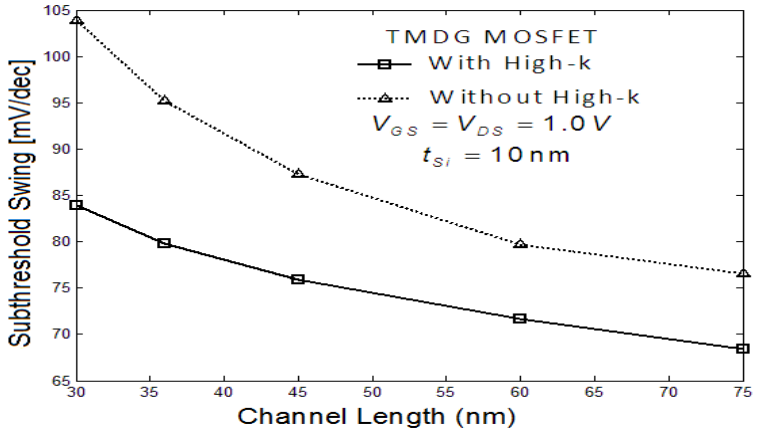

Figure 10. Subthreshold swing vs channel length of TMDG MOSFETs with and without high-k dielectric for the Silicon film thickness of t_{Si}=10 nm and V_{DS}=V_{GS}=1.0 V

Perfect scaling of channel thickness ensures the volume inversion and thus the device performance is better than the MOSFETs with high-k. An increased electric field and electron density at source side of the TMDG MOSFETs with high-k device (Fig. 4, Fig. 5 and Fig. 6) causes more rapid acceleration of carriers in the channel of the device [7].

4. Conclusions

To reduce the short-channel effects (SCEs) and hot electron effects (HCEs) of nano-scale double-gate MOSFETs, to solve the gate oxide scaling problem and improving the reliability of the device, a triple material double-gate (TM-DG) MOSFET,with high-k dielectric (HfO_2) in the gate oxide (along with SiO_2) is proposed. TM-DG MOSFETs with high-k dielectrics gives improvements in almost every respect such as improved transconductance, subthreshold swing and OFF state current. Better reduction of SCEs and an improvement in the device reliability has been observed through the 2D simulation results by proper tuning of the channel thickness to ensure the volume inversion.

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