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Study of Silicon Body Thickness and Channel Length on SCEs and Electrical Performances of Underlapped GS-DG-MOSFET

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Abstract

In this paper, the investigation is carried out with the variation of silicon body thickness (T_{Si}) and channel length (L_G) of underlap gate stack (GS) on double-gate MOSFET (DG MOSFET) using Sentaurus TCAD Simulator. The device performances Sub-threshold Slope (SS), the threshold voltage (V_{TH}), the Switching current ratio (I_{ON} and I_{OFF} ratio), Potential energy, Electric Field and Electrostatic potential are discussed. Additionally, the analysis highlights the reduced Short Channel Effects (SCEs) and suggest the possibility for good electrical behavior of the device and therefore simulation results been taken with the T_{Si} = 7 nm with SS = 63 mV/decade and I_{ON}/I_{OFF} ratio= 10^6, and at L_G= 30 nm the SS = 60 mV/decade and I_{ON}/I_{OFF} ratio = 10^5 are observed.

Keywords: *Underlapped Gate Stack-Double Gate-MOSFET, high-k, SCEs and Electrical performances, TCAD*

1. Introduction

The advancement of technology in the new era fulfills the demand of low power applications of the MOS devices with enhanced performance and speed for integrated circuit (IC) design. So the device design enters towards nanoscale regime even with various fabrication related issues and Short Channel Effects (SCEs). The device performance degradation occurs due to the process dependent fluctuations of the device parameters such as the body (T_{si}) and channel length (L_G). Mostly it is highly desirable to explore the pre-fabrication device performances variation apropos of above two parameters.

The prediction of pre-fabrication device performance through simulation is of paramount importance for IC designer. The key performances such as Sub-threshold Slope (*SS*) [1], Threshold Voltage (V_{TH}) and the Switching ratio (I_{ON} and I_{OFF} ratio) [2] need to be analyzed at nanoscale devices. The Underlapped Gate-Stack Double-Gate MOSFET (U-GS-DG-MOSFET) has proven to be quite effective in reducing the SCEs among from numerous nanodevices proposed [3]. To achieve high performance of the device, the on current (I_{ON}) should be high in a scaled device. Due to the scaling, a thin gate oxide thickness (T_{ox}) [4] leads to the gate leakage current [3], [5], [6]. As per the International Technology Roadmap of Semiconductor (ITRS), T_{ox} is responsible for controlling the gate tunneling effects [7]. To overcome the tunneling effects, the gate insulators with dielectric (high-k) materials which can be replaced with of silicon dioxide (SiO_2) [8]–[11]. To overcome the issue of scattering due to high-k dielectric material [12]–[14], the interfacing or padding layer is introduced known as Gate Stack (GS) which thereby enhance the electric field across the channel [5], [15], [2].

This paper reports on the SCEs and the electrical parameters of the U-GS-DG-MOSFET. The simulation result is carried out to analyze the device effectiveness with T_{Si} and L_G variation using the Sentaurus TCAD simulator [16]. The impact on SCEs such as

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SS, I_{ON}, I_{OFF} and the electrical parameters like Doping Concentration, Electric Field Density, and Band diagram, Electrostatic Potential are observed by variation of the T_{Si} and L_G of the device. Along with the introduction, Section 2 discusses the device design and the simulation methodology. In Section 3, the result discussion includes the performance analysis of U-GS-DG MOSFET. Finally, the conclusion is drawn.

2. Device Design and Simulation Methodology

The device U-GS-DG-MOSFET with source/drain underlap regions has been designed concerning ITRS technology parameters [7], [17] listed in Table 1 [18]. The Figure. 1(a), and 2(a) describe, $L_{EFF} = L_G + L_{US} + L_{UD}$ where L_G is the length of the gate, L_{US} is the length of the Source underlap region, L_{UD} is the length of the Drain underlap region, and the L_{EFF} is the gate conductivity region of the channel region of the device [8], [19]–[22]. In the device, physical gate height is increased the by the use of HfO_2 (high-k), an interfacial layer of SiO_2 with same Effective Oxide Thickness (EOT). For the isolation purpose, the EOT of 0.9 nm is considered with GS of T_{OX1} and T_{OX2} (SiO_2 and HfO_2) [8]–[11].

Table 1. Device Parameters Considered for the Simulation Framework

Parameters	**U-GS-DG-MOSFET**	**U-DG-NMOSFET with Gate Stack** [18]
N^+-type (Arsenic Doping Concentration) at source/drain regions	10^{20} cm^{-3}	10^{20} cm^{-3}
P-type (Boron Doping Concentration) at channel region	10^{15} cm^{-3}	10^{15} cm^{-3}
Gate length(L_G)	18, 30, 70, 120 nm	18 nm
Effective Channel Length($L_{EFF}=L_G+L_{US}+L_{UD}$)	58, 70, 140, 160 nm	58 nm
Effective Oxide Thickness(EOT)	0.9nm	0.9nm
Silicon Body thickness(T_{Si})	7, 10, 15, 20 nm	16 nm
The thickness of SiO_2 layer (T_{OX1})	0.45 nm	0.45 nm
The thickness of HfO_2 layer (T_{OX2})	2.9 nm	2.9 nm
Gate Thickness(T_G)	10 nm	10 nm
Work Function(ϕ_M)	4.3 eV	4.3 eV

The schematic view of U-GS-DG-MOSFET represents the doping concentration of constant L_G with varying T_{Si} as shown in Figure 1(a), and another analysis is done by making L_G variable keeping T_{Si} constant shown in Figure 2(a).

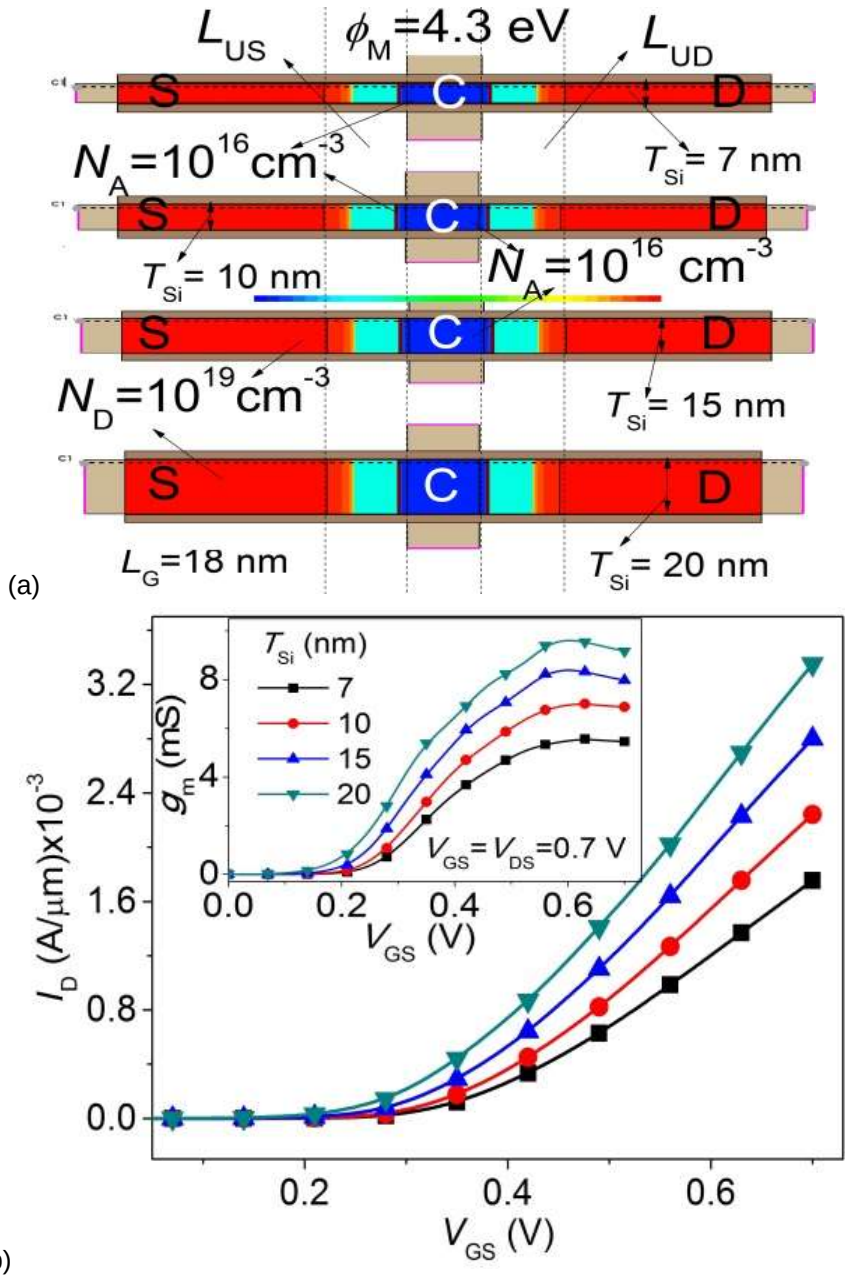


Figure 1. (a) Schematic View of GS-DG MOSFET with Different T_{Si} Values, (b) I_D-V_{GS} Characteristics and the Inset Figure Represents the g_m-V_{GS} at L_G=18 nm

The Figure 1 (b) and Figure 2 (b) shows the I_D-V_{GS} graphs which represent the transfer characteristics and the transconductance (g_m). The characteristics graphs for both the designs (by varying T_{Si} and L_G for different drain voltages (0.05 V and 0.7 V). As shown in the figure, the increased value of T_{Si} increases the I_{ON} and the g_m values. Accordingly, due to the variation in L_G (the increased value) decreases the I_{ON} and the g_m values.

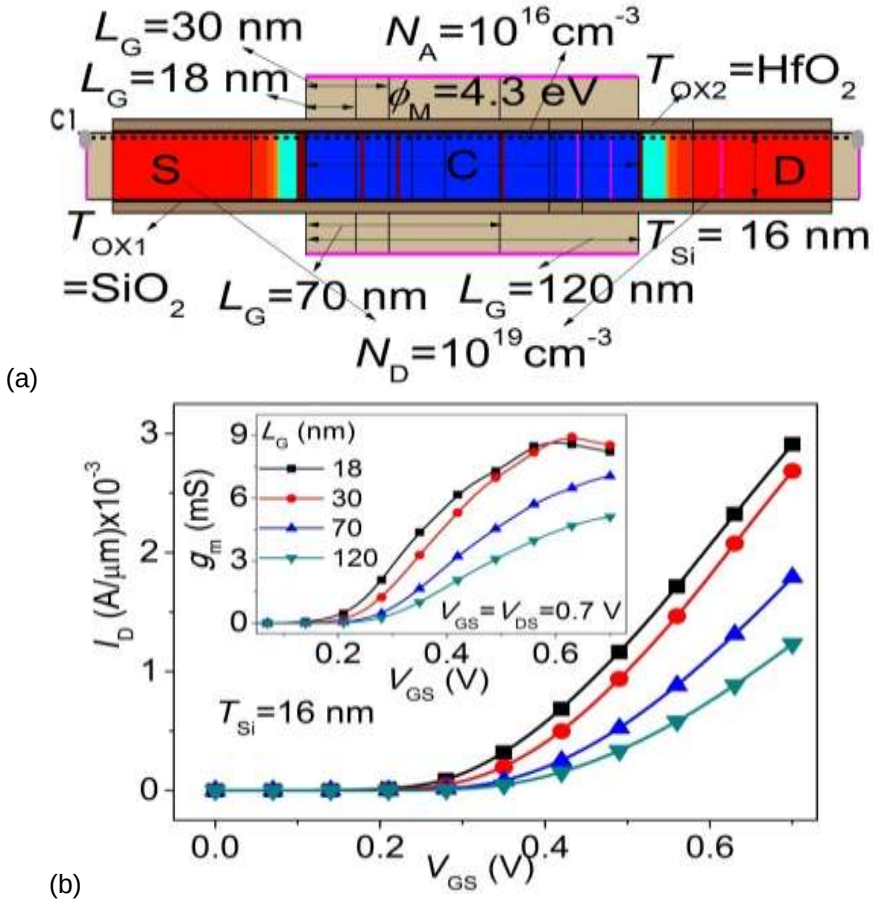


Figure 2. (a) Schematic View of GS-DG MOSFET with Different L_G Values, (b) I_D-V_{GS} Characteristics and the Inset Figure Represents the g_m-V_{GS} at T_{Si}= 16 nm

The simulation is carried out by using TCAD simulator to study different performances of the device [16]. The simulation is carried out by activating Arora mobility model [23]. This model used to describe the carrier mobility degradation due to the Coulomb scattering effect [24]. The doping dependent model describes the carrier velocity which works under the saturation with the impact of the high electric field [18] [25]. The drift-diffusion model is taken into account for the carrier transport, and the Shockley-Read-Hall (SRH) [26] recombination model is used to include the carrier generation and recombination model [18][27]. Furthermore, the simulation is incorporated using the enhanced Lombardi model for the study of the effect of high-K mobility degradation of the carrier in the silicon inversion layer [28].

3. Results and Discussions

In this Section 3 1 the study of the impact on the SCEs and in Section 3 2 the effect on the Electrical Parameters has been analyzed.

3.1. Impact of L_G and T_{Si} on Short Channel Effects (SCEs)

The SCEs are important to consider when the device enters to the nanoscale regime. The simulation of the device is done by varying T_{Si} (keeping the L_G constant) and by varying the L_G (keeping the T_{Si} constant). In Figure. 3(a) and 3(b) it is shown the I_{ON} and I_{OFF} ratio increases with increased values of the channel length and T_{Si}. By comparing

both the variation, it is understood that the T_{Si} variation gives a better result for the I_{ON} and I_{OFF} ratio. The Sub-threshold Slope (*SS*) is defined for the long-channel devices. The Sub-threshold current is independent of the drain voltage but is dependent on the gate voltage exponential for larger values, hence the inverse of the $\log_{10}$ (I_{DS}) versus V_{GS} characteristic is called the Sub-threshold Slope (*SS*). The *SS* of the device is shown in the inset figure below in Figures 3(a) and 3(b). The *SS* value increases with the increase of the $T_{Si,}$ but the *SS* value decreases with the increase of L_G. Henceforth, the two results obtained are near to the ideal values of standard MOSFET. The I_{ON}-I_{OFF} ratio and *SS* tends to saturate at L_G =20nm (T_{Si} (constant) =16 nm) and T_{Si} =20 nm (L_G (constant) =18nm). The SCEs is observed when the V_{GS}=V_{DS}= 0.7 V (saturation point of the MOSFET operating voltage).

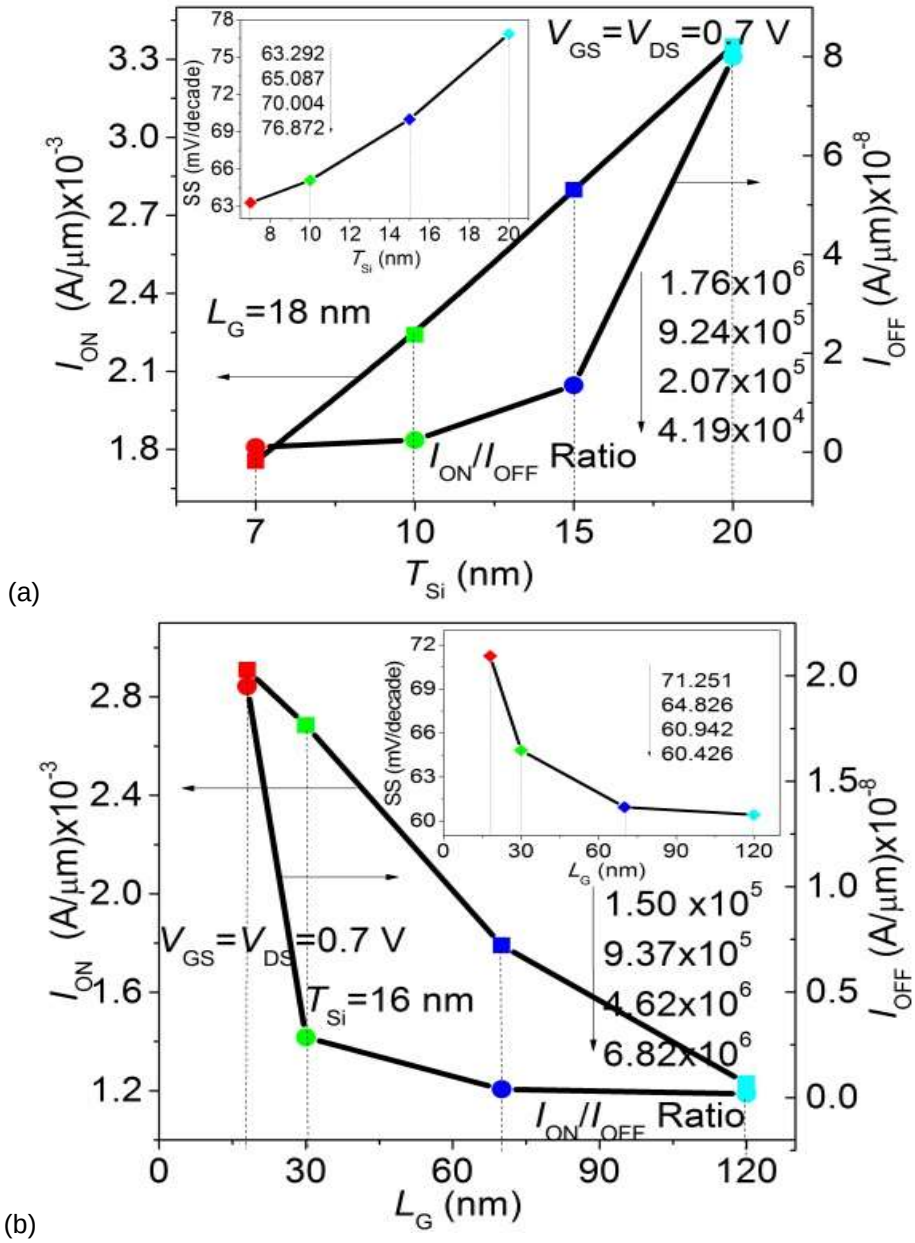


Figure 3. (a) I_{ON} and I_{OFF} as Function of T_{Si} Variation at L_G=18 nm, (b) I_{ON} and I_{OFF} as Function of L_G Variation at T_{Si} =16 nm and the Inset Figure for both (a) and (b) Represents Sub-threshold Slope (*SS*)

3.2. Impact of Electrical Performance on U-GS-DG MOSFET

3.2.1. Impact of Electrical Performances with T_{Si} Variation

The analysis is made at saturation voltage at V_{GS}=V_{DS}= 0.7 V and after taking the 2D cutline across the oxide channel interface for different T_{Si} values the electrical performances are observed. The Figures 4(a), 5(a) and 6(a) shows the Electrical parameters of U-GS-DG-MOSFET for the Potential Energy, Electric Field and the Electrostatic potential with the T_{Si} variation and the plotting of respective graphs are shown in Figures 4(b), 5(b) and 6(b).

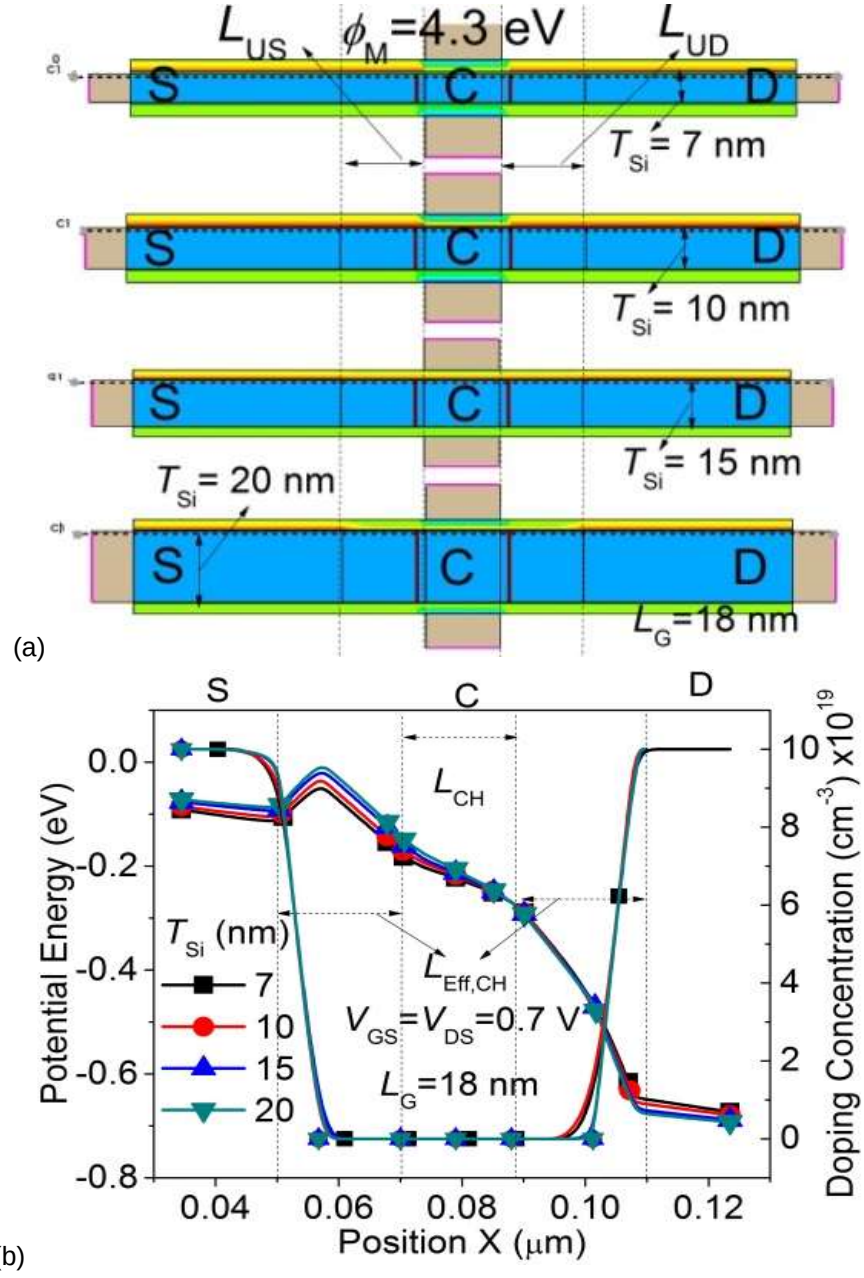
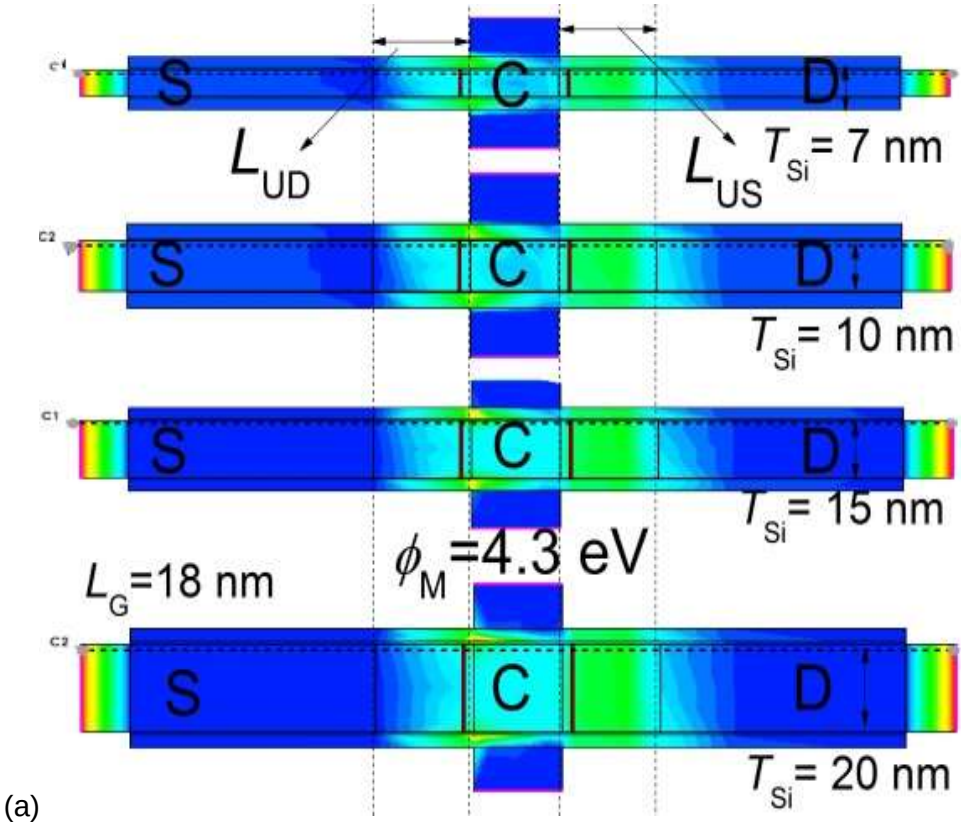
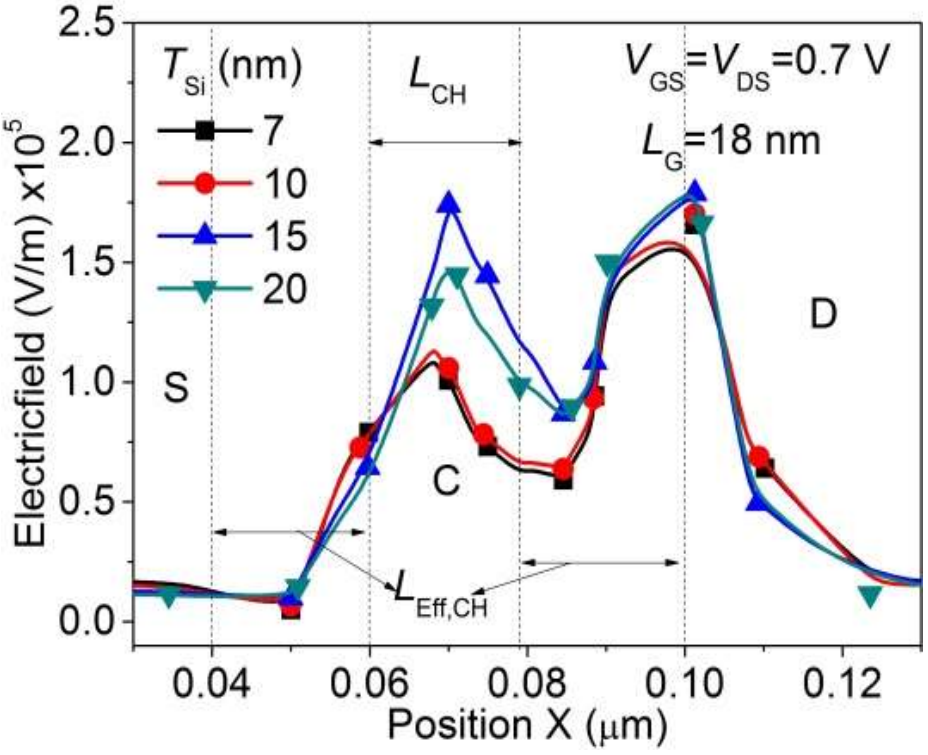


Figure 4. (a) 2D Representation of Potential Energy, (b) Potential Energy and Doping Concentration as a Function of Position 'X' at L_G=18 nm for Different T_{Si} Values



(a)



(b)

Figure 5. (a) 2D Representation of Electric Field, (b) Electric Field as Function of Position 'X' at L_G=18 nm for Different T_{Si} Values

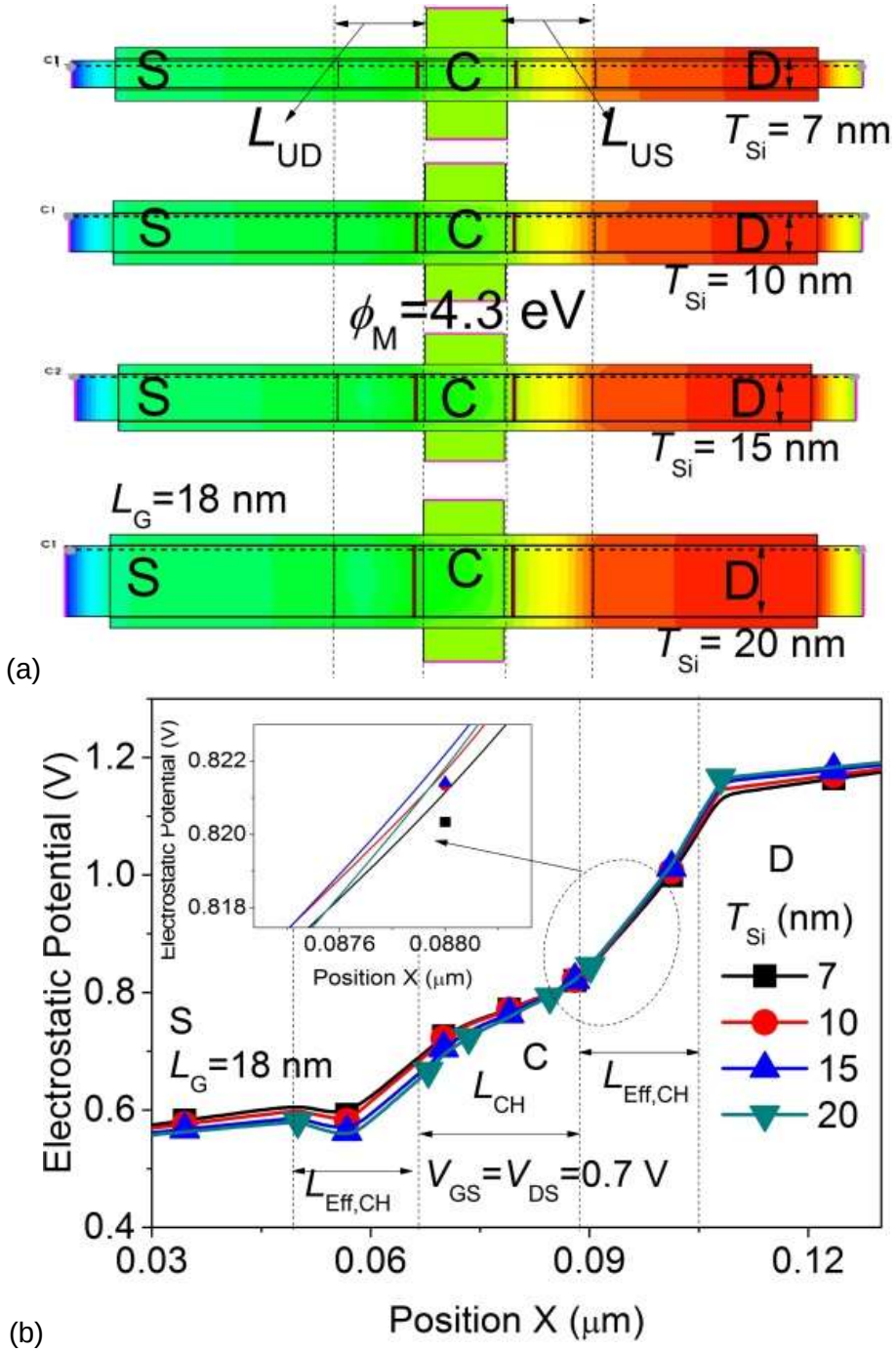


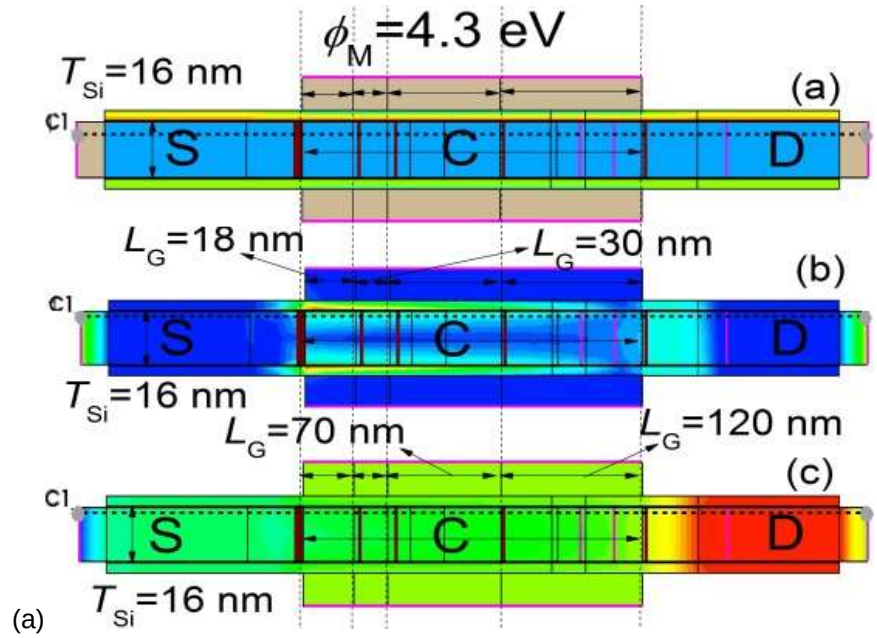
Figure 6. (a) 2D Representation of Electrostatic Potential, (b) Electrostatic Potential as Function of Position 'X' and Inset Figure Shows the Encircled Region at L_G=18 nm for Different T_{Si} Values

In this section, the performances of the Electrical parameters represented graphically. In Figure 4(b) the representation of the potential energy and the doping concentration with different values of T_{Si} are shown, and the parameters found out to be symmetric to the ideal MOSFET[1]. The Doping concentration remains unchanged throughout the device dimensions, so due to this reason the conduction band showing an increasing notch at the L_{UD} region and it has almost zero Electric field at the source side, so the density of the Electric field is more near Drain side. The variation in the density of the Electric field which changes from channel towards the Drain side, at the peak value of channel towards

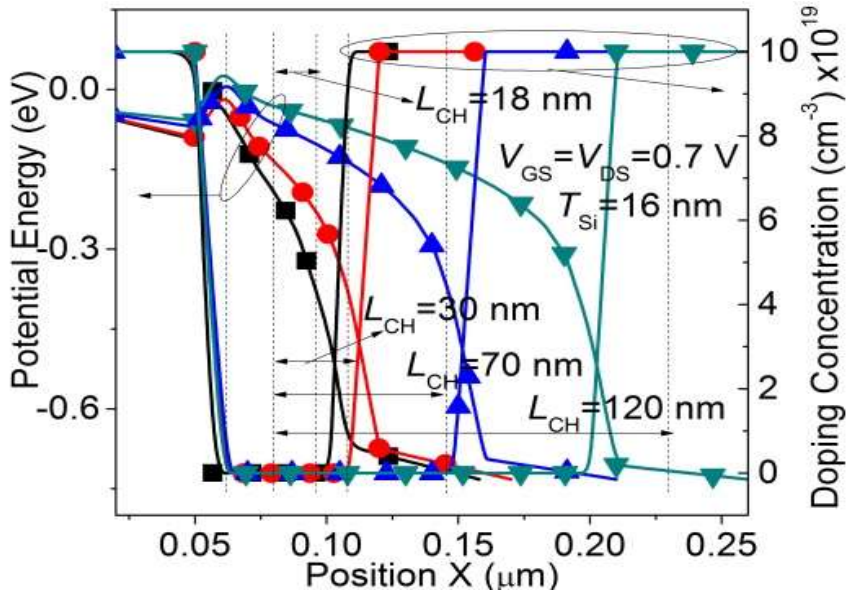
Drain Region is shown in Figure 5(b). The change in the Electric field occurs as the thickness increase in case of T_{Si} variation. As per the Figure 6(b), at the maximum biasing voltage the high Electric field is observed towards the Drain region. Similarly, the variation in Electrostatic potential is found by moving from Source side towards Drain side.

The surface potential is no longer symmetrical in this regime, due to channel potential. The minima of the parabola are shifted towards the source side instead of being near to the mid of the channel is shown in Figure 6(b) for T_{Si} variation and in Figure 7(d) for L_G variation. Therefore, the scaling channel length affects the shifting in the minima of the potential and also change in the V_{TH} value.

3.2.2. Impact of Electrical Performances with L_G Variation



(a)



(b)

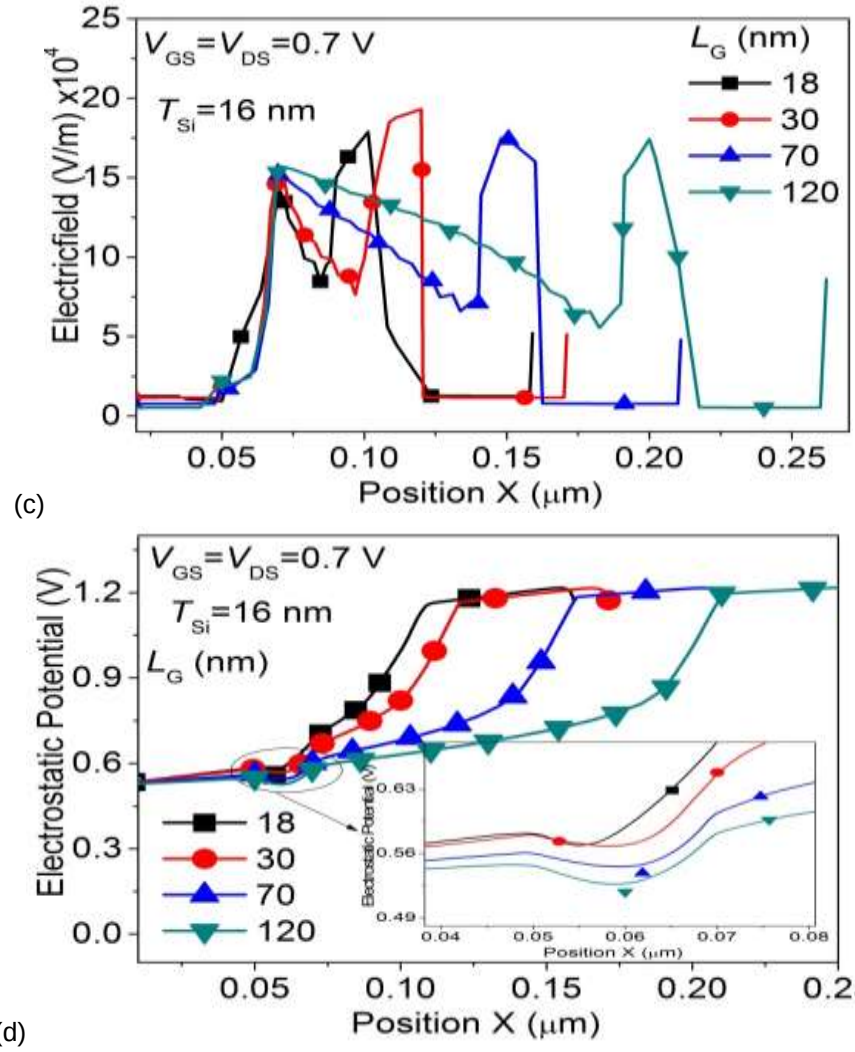


Figure 7. (a) 2D Representation of Potential Energy, Electric Field, and Electrostatic Potential, (b) Potential Energy and Doping Concentration, (c) Electric field, (d) Electrostatic Potential as a Function of Position 'X' at T_{Si} =16 nm for Different L_G values

In Figure 7(a) the 2D representation of Potential Energy, Electric field, and Electrostatic Potential has been shown. In Figure 7(b) it is shown that as the channel length increases, the band bending occurs more in the channel region. Hence the Potential Energy increases for more substantial L_G value at T_{Si} =16 nm. As the L_G values increase the Electric field and Electrostatic Potential also increases in mid of the channel region, L_{UD} and in the Drain region as shown in Figures 7(c) and (d).

4. Conclusion

In this study, a systematic investigation of U-GS-DG-MOSFET is carried out with the variation of the silicon body thickness and channel length. It is observed that T_{Si} and L_G variation has a significant effect on device performances. The analysis shows the reliable performances of the device for the reduced SCEs and good electrical performance parameters. Thus the impact of the GS and Underlapped region features to enhance the device performances with *SS*, I_{ON} and I_{OFF} ratio which is emerging as the better option as projected by the results of the device and also summarizes that further study can be done in GS engineering.

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