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Design and Implementation of 8-Bit Low Power Parity Preserving Carry Skip Adder Using Reversible Computing

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Abstract

The fundamental operation in most digital circuits is binary addition. It serves as a building block for synthesis all other arithmetic operations. Low-power and high-speed adder cells (like carry skip adder) are used in binary operation based devices. Now the biggest challenge is reduction of adder circuit power consumption and maintaining the high performance in different types of circuit design. Parity preserving is also one of the oldest methods for error recognition in digital systems. In this article 8-bit & modified 8-bit design of carry skip adder is proposed. The proposed method uses gates such as ZPLG, LCG, NFT & F2G reversible logic gates as skip logic in the design that leads to decrease in power consumption & quantum cost of the circuit.

Keywords*: Reversible Logic, ZPLG Gate, Carry Skip Adder, Quantum Cost, Power Consumption*

1. Introduction

Power and speed is an important term in low power VLSI circuit design. There are some conventional methods to optimize the power and speed such as reducing switching activity, lower power supply and reducing technology of the devices. These methods are not fulfilling the criteria to meet present scenario of power optimization. The classical digital approach has been used the digital logic gates, which are irreversible in behaviour. These irreversible digital gates generate energy due to the bit loss during computation. Bit loss occurs because the input and output vector are not equal in number. Thus, classical digital logic dissipates heat for every bit loss during computation (Landauer 1961) more precisely bit loss dissipate kT ln2 joule of energy where k is Boltzmann's constant and T is the temperature at which computation operation performed [2]. According to Bennett in 1973 proves that in order to nullify the energy loss it is essential that all logic computation operate to be in a reversible logic way [1]. Thus, every latest technology has to use reversible gates in order to power and delay optimization

2. Basic Reversible Gates

Reversible gates are n*n logic gates where the input vectors I = I(i1; i2; : : : ; in) are mapped to the output vectors O = O(o1; o2; : : : ; on).

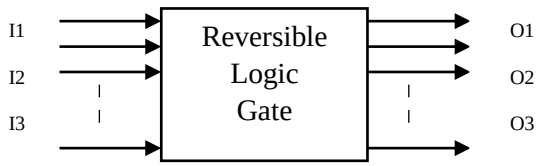

Figure 1. Block Diagram of Reversible Logic Gate

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The mapping is bijective, *i.e.*, every input is mapped to an output and every output has a unique input mapped to it. Thus the outputs of reversible gates are permutations of the inputs. Fan-outs are not allowed in reversible circuit since they violate one-to-one mapping. Some basic reversible gates are introduced in this section.

2.1. LCG Gate

LCG gate is a low complexity gate. It has a very low hardware complexity. It has a quantum cost of 10. This gate is used to construct a low-cost parity preserving full adder. The block diagram of LCG is illustrated in Figure 2.

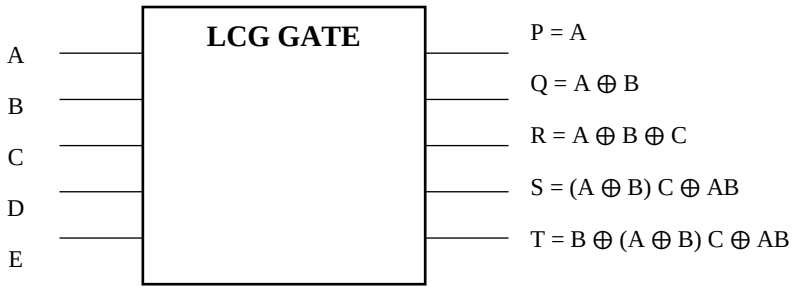

Figure 2. Block Diagram of LCG Gate

2.2. ZPLG Gate

ZPLG gate is 5*5 gate. The ZPLG gate can be used as parity preserving if we set the inputs D & E to zero. It has a quantum cost of 8. This gate is also used to construct a low-cost parity preserving full adder. The block diagram of ZPLG is illustrated in Figure 3.

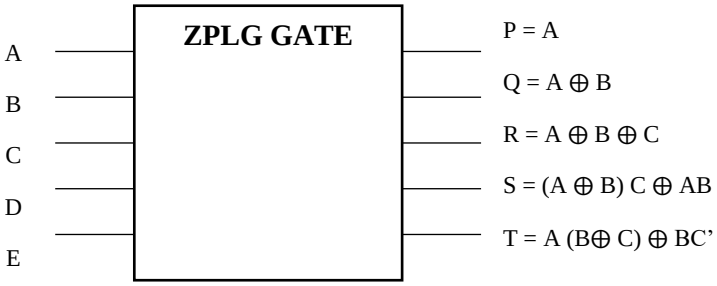

Figure 3. Block Diagram of ZPLG Gate

2.3. F2G Gate

It is a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The outputs are defined by P = A, Q = A ⊕ B, R = A ⊕ C. Quantum cost of Double Feynman gate is 2.

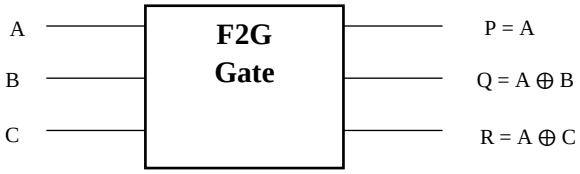

Figure 4. Block Diagram of F2G Gate

2.4. NFT Gate

New fault tolerant gate (NFT) is a 3*3 parity-preserving reversible gate. NFT gate is able to implement all Boolean functions of AND, XNOR, NAND, XOR, NOR, and NOT. Quantum cost of NFT gate is equal to 5.

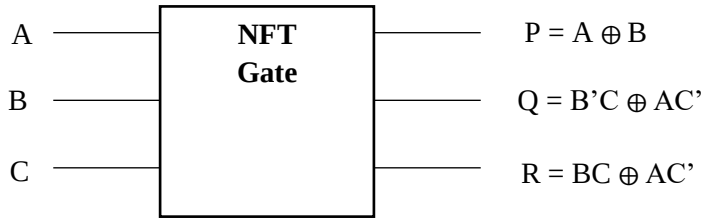

Figure 5. Block Diagram of NFT Gate

3. Literature Survey

In 1961, R. Landauer described that the logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In conventional system the millions of gates used to perform logical operations. The author proved that heat dissipation avoidable if system made reversible [1].

In 1973, C.H. Bennett described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Reversible gate can generate unique output vector from each input vector and vice-versa [2].

In 2011, Md. Mazder Rahman *et al*. presented a quantum gate library that consists of all possible two-qubit quantum gates which do not produce entangled states. These gates are used to reduce the quantum cost of reversible circuits. They proposed a two-qubit quantum gate library that plays a significant role in reducing the quantum cost of reversible gates [3].

In 2012, B. Raghu Kanth *et al*. described the comparison between the reversible and conventional logic gates. The authors compared the 4-bit reversible adder/subtractor circuit using DKG gate. The comparison is carried out in terms of low power consumption, lesser delay, number of gates, garbage outputs and constant inputs. The results of this adder/subtractor circuit using DKG gate was better as compared to existing one and this adder/subtracted circuit can be applied to the design of complex systems in nanotechnology. The authors demonstrated that a 4*4 reversible DKG gate can work singly as a reversible full adder and a reversible full subtraction [4].

In 2013, Partik Kumar Bhattdescribed the reversible comparator which is implemented with the Reversible BVN gate. The design is very useful for the future computing techniques like ultra-low power digital circuits and quantum computers. The implementation of this comparator has advantages of reducing the number of garbage outputs, gate count and number of constant input and quantum cost [5].

In 2014, A. Anjana designed the RS Flip-Flop using Reversible logic gate which is implemented by cascading the Toffoli gate and TNORG gate.By using reversible logic gates power consumption was estimated 52mW & path delay was about 6.991ns which was very less as compared to using conventional gate. The number of gates is reduced from 6 to 2 as compared to the existing module [6].

In 2014, Ashima Malhotra *et al*. proposed different types of reversible multiplexers using modified Fredkin gates. They proposed 2:1, 4:1, 8:1 and 16:1 reversible multiplexers. They also compared the quantum cost and power consumption of proposed reversible multiplexers with previous designs [7].

In 2014, Ashima Malhotra *et al*. described that reversible modified Fredkin gate used to design the multiplexers with low quantum cost and compare it with existing work. They compared the quantum cost of multiplexers design using Fredkin gate with Modified Fredkin gate used to design he multiplexers [8].

In 2015, Sukhjeet Kaur *et al*. proposed different types of reversible encoders using Feynman and Fredkin gates. They proposed 4:2, 8:3 and 16:4 reversible encoders. They also compared quantum cost of proposed reversible multiplexers with previous designs [10].

In 2015, Manjinder Pal Singh*et al*. proposed different types of reversible decoders using BVF, F2G and FRG gates. In this paper, 2:4, 3:8 and 4:16 reversible decoders were proposed. The quantum cost and hardware complexity of proposed reversible multiplexers has been reduced as compared to previous designs. The reversible logic circuits can also be designed with less area and delay [11].

In 2016, Ankush *et al*. described that the reversible modified Fredkin gates and modified HNG gates can be used to design the Carry Skip adder with low quantum cost. The quantum cost and the power dissipation of proposed carry skip adder design using modified Fredkin gates was reduced as compared to existing carry skip adder using Fredkin gate [12].

In 2016, Ankush *et al*. proposed different types of reversible residue adders using modified Fredkin gates and modified TSG gates. Various parameters of reversible circuits such as, quantum cost and power dissipation of proposed reversible residue adderswere reduced as compared to previous designs. The reversible logic circuits can also be designed with less area and delay [14].

In 2017, Palak, *et al* proposed different types of 8-bit reversible parity preserving carry look ahead adder using fredkin gate, modified Fredkin gate and F2G gate. They compared parameters *i.e.* quantum cost and power consumption of proposed reversible carry look ahead adders with existing one. The reversible logic circuits can also be designed for n-bit crcuit. [15].

In 2017, Ankush *et al* described the improved design of Low power BCD adder which is implemented using MTSG, NG & Feynman gates. This BCD adder is specially designed to make it suitable for the reversible logic implementations. This design strategy reduces the most important factor of the reversible circuit quantum cost and the power consumption of the circuit. [16].

In 2017, Roop Shikha *et al*. described that reversible ZPLG gate used to design the parity preserving ripple carry adder with low quantum cost and compare it with existing work. They compared the quantum cost of parity preserving ripple carry adder design using LCG gate with ZPLG reversible logic gate used to design the low power party preserving ripple carry adder [17].

In 2017, Ankush *et al*. proposed the low power reversible multiplier circuit which is implemented with the Reversible MHNG gate. The design is very useful for the future computing techniques like ultra-low power digital circuits and quantum computers. The results of this low power multiplier circuit using MHNG gate was better as compared to existing design using HNG gate and this reversible multiplier circuit can be applied to the design of complex systems in nanotechnology [18].

4. Proposed Work

The following figure shows the block diagram of the proposed 8-bit carry skip adder using LCG, NFT & F2G gates.

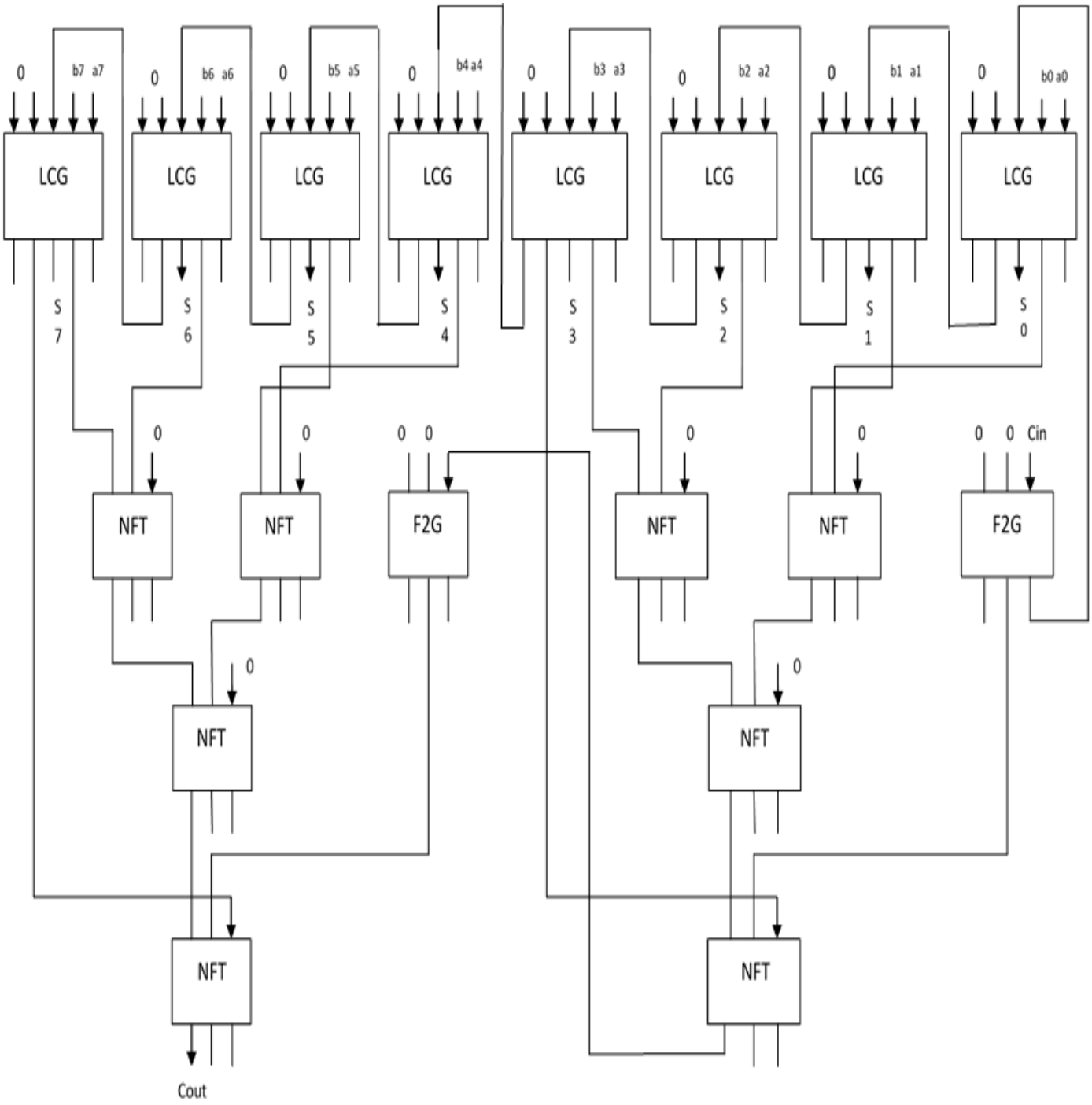

Figure 6. Proposed Design of 8-bit CSA

The following figure shows the block diagram of the Modified proposed 8-bit carry skip adder using ZPLG, NFT & F2G gates.

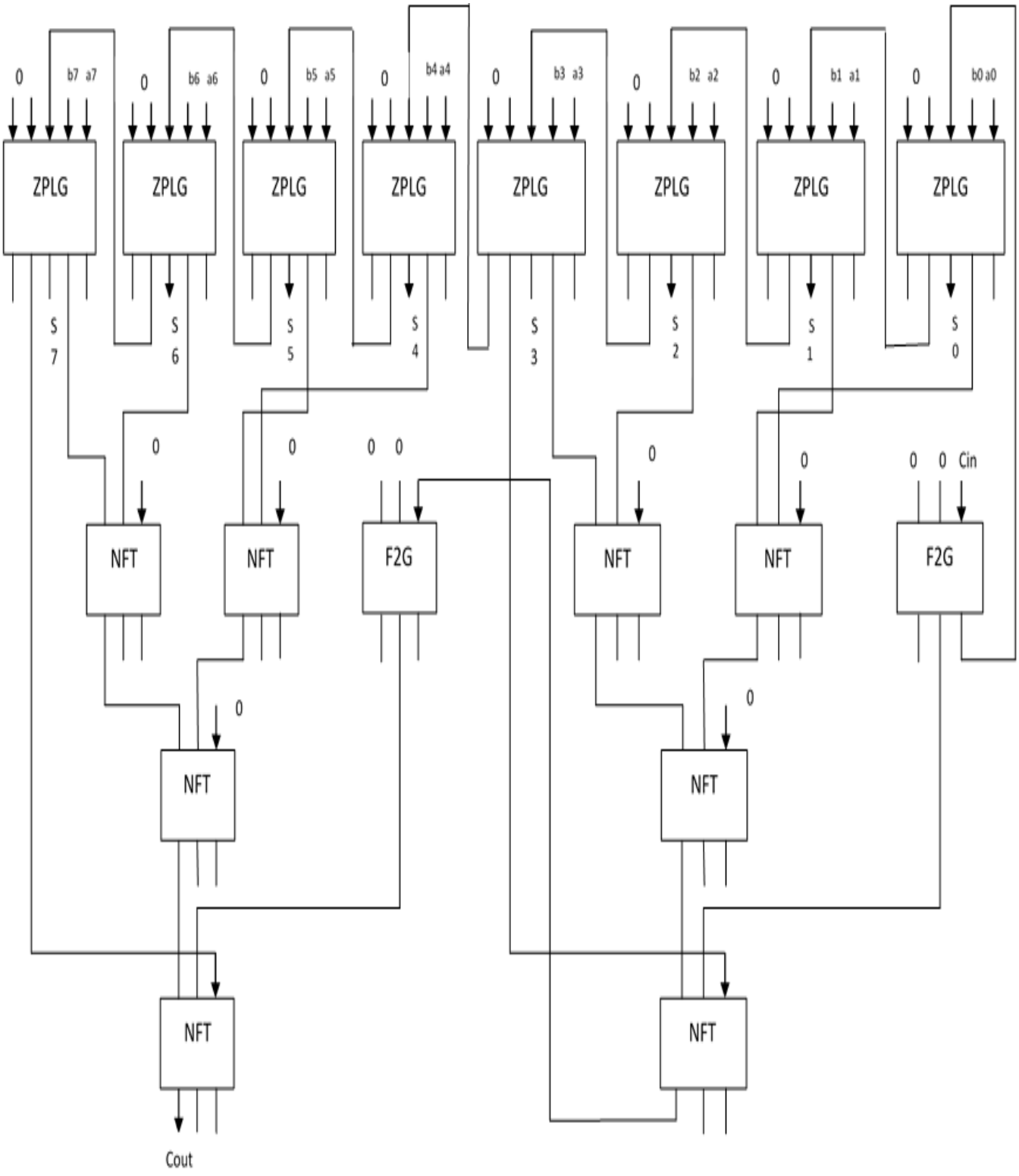

Figure 7. Proposed Design of 8-bit Modified CSA

The Figure 6 & 7 shows the block diagram of proposed & modified proposed 8-bit carry skip adder using various reversible logic gates. Low power adder circuits have become very important in VLSI industry. Adder circuit is one of the main building block in DSP processor. Adder is the main component in most of the arithmetic unit. Addition is

a fundamental operation for any digital system, DSP or control system. The fast operation of a digital system is having great influenced by the performance of the resident adders. Adders plays important Component in digital systems because of the more number for use in other basic digital operations such as subtraction, multiplication and division. Hence, the improving performance of the digital adder increases the execution of various binary operations in a circuit consisting of different blocks. The appearance of the digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed. There are many works on the subject of optimizing the speed and power of these units, which has been reported. Obviously, it is extremely possible to achieve higher speeds at low-power and energy consumptions, which is one of the challenges for the designers of general purpose processors. The carry skip adder is one of the fastest adders used in many digital processors to perform arithmetic operations.

The Figure 6 shows the proposed design of 8-bit reversible carry skip adder using F2G, LCG & NFT gates. In this design there are total 8 LCG gates used which serves as a parity preserving gate & Full adder circuit. Each LCG gates accepts two inputs a and b and provide one sum output S. The quantum cost of LCG gate is 10. Here the gates used LCG & NFT are the parity preserving gats. The parity preserving is one of the simple but efficient characteristics that make a reversible circuit fault-tolerant. Thus, it is beneficial to make the gates or circuits fault-tolerant in the form of parity preserving. The parity preserving characteristic, the used fault model in the parity preserving reversible circuits is the logical fault model in which the output deviations at the logic level are considered not taking the cause of faults into account. Thus the total quantum cost of the proposed design 2nd is given below:

$$\begin{aligned} \text{QC (Proposed Design)} &= 2\ \text{QC (F2G)} + 8\ \text{QC (LCG)} + 8\ \text{QC (NFT)} \\ &= 4 + 80 + 40 \\ &= 124 \end{aligned}$$

The Figure 7 shows the proposed modified design of 8-bit reversible carry skip adder using F2G, ZPLG & NFT gates. To reduce the quantum cost of the proposed design 2nd the modified form is designed. In this design there are total 8 ZPLG gates used which serves as a parity preserving gate & Full adder circuit. A parity preserving full adder requires at least two constant inputs and three garbage outputs. According to Figure 8, the ZPLG performs the add operation on the inputs A, B and C, and produces the corresponding outputs, sum and carry (Cout), as required. In this Figure 8, it should be noted that the output logic equation for Cout = ((A ⊕ B) C ⊕ AB) is the same as the ordinary logic AB + AC + BC for the output carry. In addition, the equality of input and output parities as required in a parity preserving full adder. Furthermore, it shows that the number of constant inputs (D and E) and the number of garbage outputs (P, Q and T) are two and three, respectively, where both are the minimum required amounts for a parity preserving full adder circuit. The total quantum cost of the proposed modified design 3rd is given below:

$$\begin{aligned} \text{QC (Proposed Modified Design 3rd)} &= 2\ \text{QC (F2G)} + 8\ \text{QC (ZPLG)} + 8\ \text{QC (NFT)} \\ &= 4 + 64 + 40 \\ &= 108 \end{aligned}$$

5. Implementation and Results

The 8-bit parity preserving CSA is designed using reversible logic and the design is analyzed on the basis of some performance parameters such as quantum cost and power consumption & compared with the proposed modified 8-bit CSA. The comparative analysis of parity preserving CSA & modified parity preserving CSA using reversible logic is shown in the Table 1 & 2 below:

Table 1. Comparison of Quantum Cost of Proposed Work with Modified Proposed Work

CSA Adder Circuit	Quantum Cost
Proposed 8-bit Design	108
Proposed Modified 8-bit Design	124

Table 2. Comparison of Power Consumption of Proposed Work with Modified Proposed Work

CSA Adder Circuit	Power Consumption (W)
Proposed 8-bit Design	4.331 W
Proposed Modified 8-bit Design	3.425 W

6. Simulation Methodology

Here, the coding is written in a VHDL language and simulated and the power is analyzed in Xilinx ISE 14.4. The Figure 8 & 9 shows the RTL schematic of top module for our proposed reversible CSA 8-bit & modified 8-bit adder circuit it contains inputs a, b each of which contains 8 bits and Cin as the input carry. The S is the output which contains 8 bits and Cout as the output carry.

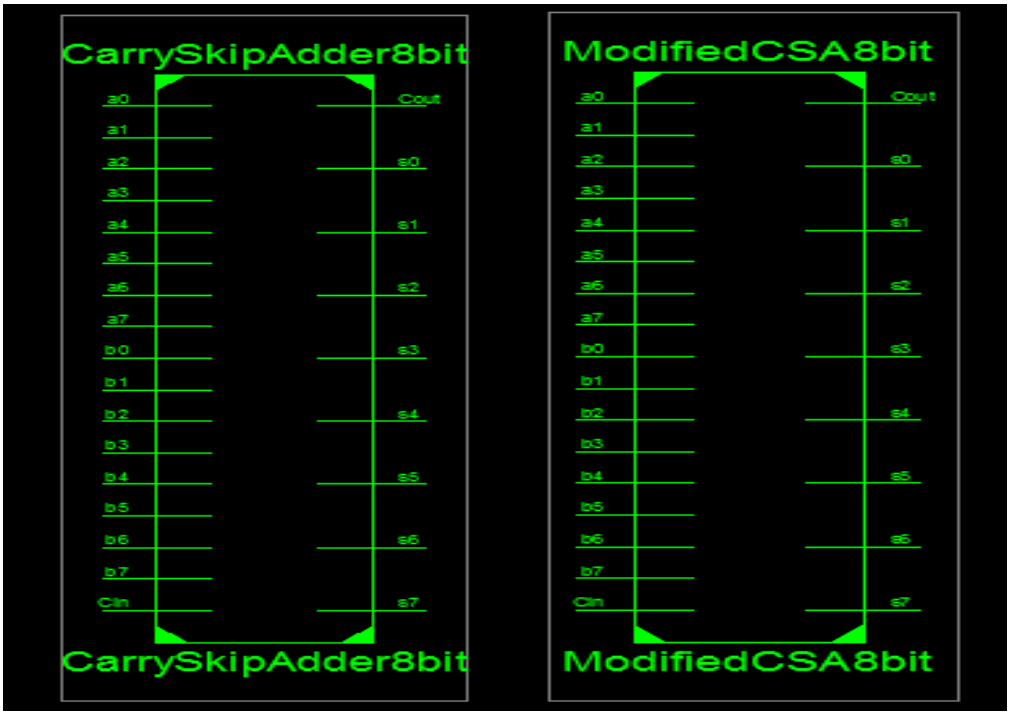

Figure 8. Block Diagram of Proposed and Modified Proposed Reversible 8-Bit CSA Adder

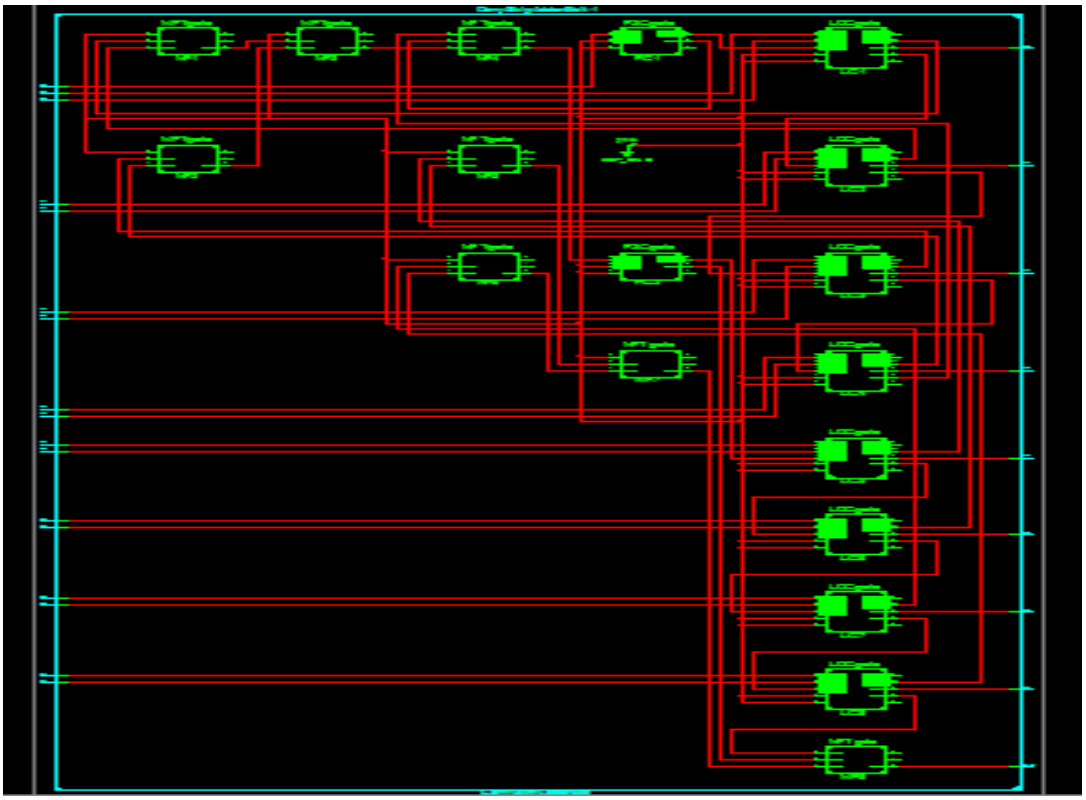

Figure 9 (a). RTL View of Proposed Reversible 8-Bit CSA Adder

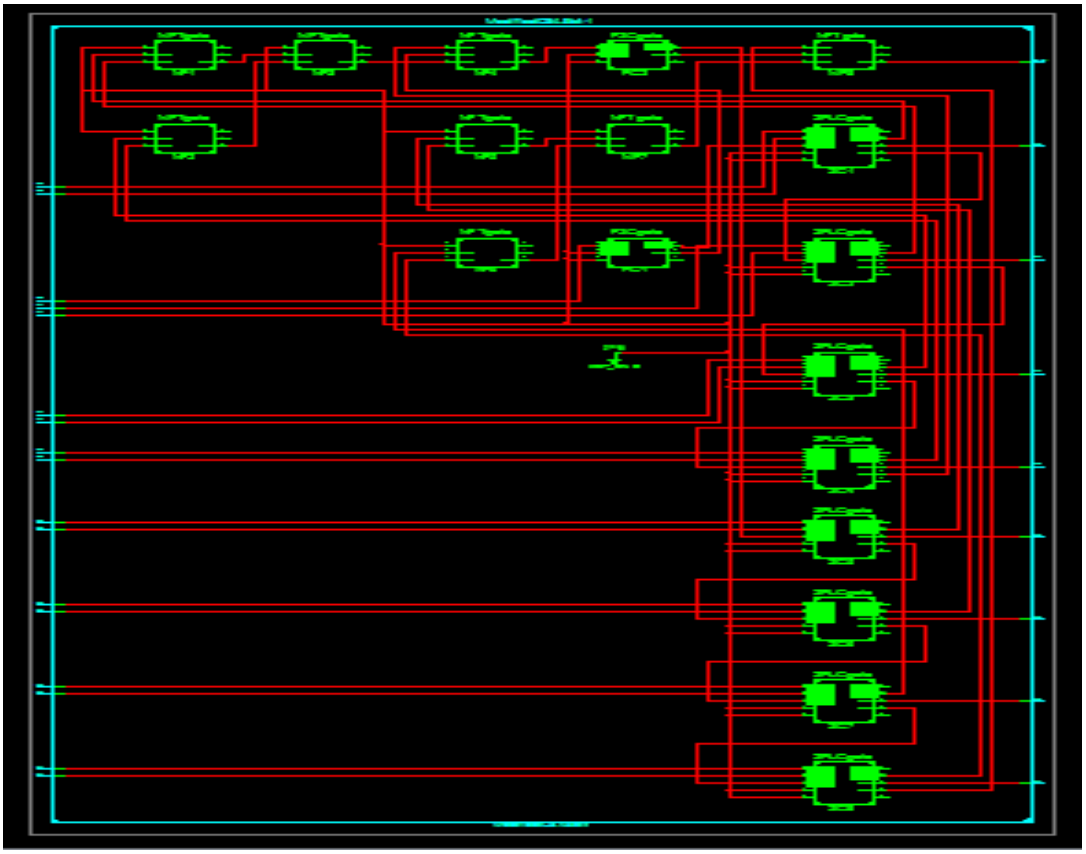

Figure 9 (b). RTL View of Proposed Modified Reversible 8-Bit CSA Adder

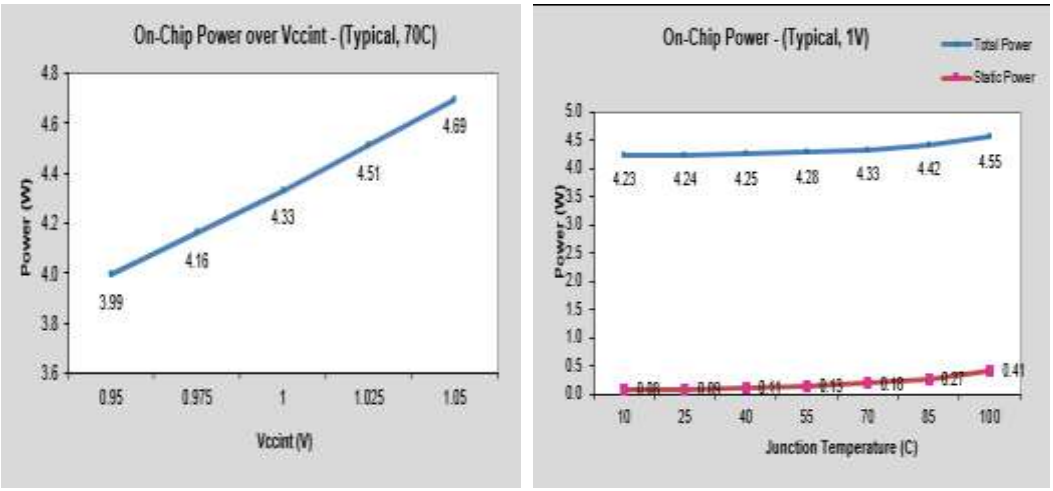

Figure 10. Power Consumption Graph for Proposed 8-bit Reversible CSA Adder

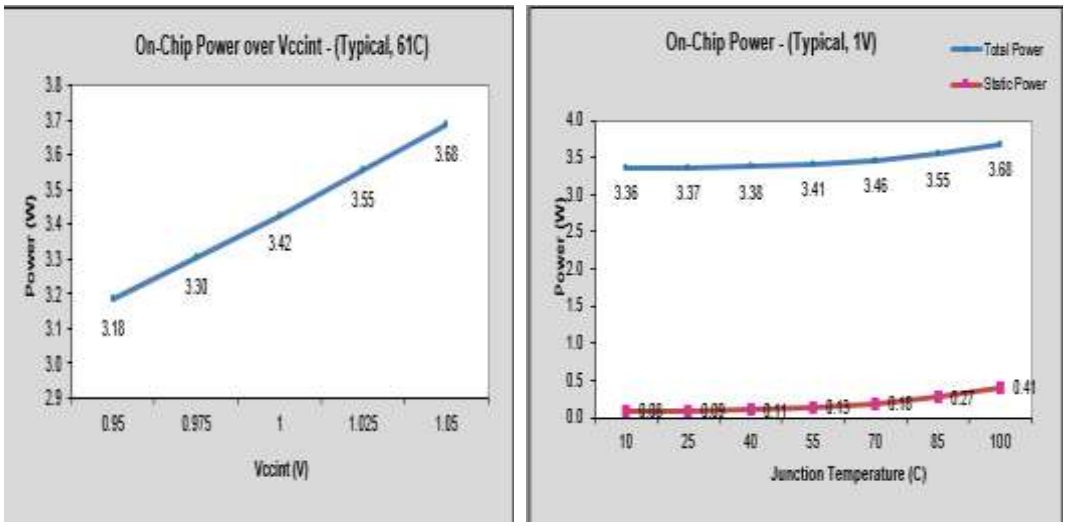

Figure 11. Power Consumption Graph for Proposed Modified 8-bit Reversible CSA Adder

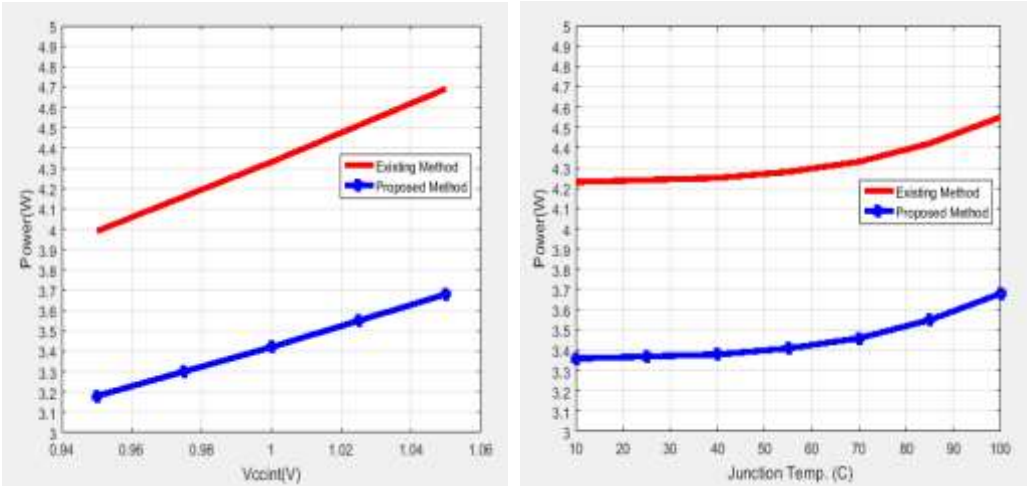

Figure 12. Comparative Results of Power Consumption Graph for Proposed and Modified Proposed 8- bit Reversible CSA Adder

It is observed that the proposed modified reversible 8-bit carry skip adder (Figure 6) is more efficient then the proposed carry skip adder (Figure 7). Evaluation of the proposed circuit can be comprehended easily with the help of the Table 1 & 2.

7. Conclusion and Future Work

The reversible logic circuits are designed to minimize the power dissipation which ultimately increase the lifetime and speed of the circuit. The researchers are attracted towards reversible logic as it has enormous applications in the emerging technologies. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a logic function will significantly impact the garbage outputs, quantum cost and power consumption of the reversible design. Further the proposed design can be implemented to design of n-bit parity preserving carry skip adder.

References

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, vol. 5, **(1961)**, pp. 183- 191.
[2] C. H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, **(1973)**, pp. 525-532.
[3] M. Rahman, "Two-Qubit quantum gates to reduce the quantum cost of reversible circuit", IEEE International Symposium on multiple-valued logic, **(2011)**.
[4] B. Raghu Kanth, "A Distinguish between reversible and conventional logic gates", International Journal of Engineering Research and Application, vol. no.2, issue no.2, **(2012)**, pp.148-151.
[5] P. K. Bhatt and A. Saxena, "Optimized Study of One-bit Comparator using Reversible Logic Gates", vol. 02, issue 09, **(2013)**.
[6] A. Anjana, "Design of RS Flip-Flop using Reversible logic Gate", International Journal of Electronics & Communication, vol. 2, issue 4, **(2014)**.
[7] A. Malhotra, C. Singh and A. Singh, "Efficient Design of Reversible Multiplexers with Low Quantum Cost and Power Consumption", International Journal of Emerging Technology and Advanced Engineering (IJETAE), vol. 4, issue 7, **(2014)**, pp 518 – 523.
[8] A. Malhotra, C. Singh and A. Singh, "Efficient Design of Reversible Multiplexers with Low Quantum Cost'', International Journal of Engineering Research and Applications, vol. 4, issue 7, **(2014)**, pp.20-23.
[9] Ankush and A. Singh Bhandari, "Review Paper on Reversible Logic Gate", International Journal for Research in Electronics & Communication Engineering, vol. 1, issue 7, **(2016)**.
[10] S. Kaur and A. Singh, "Design and Performance Analysis of Encoders using Reversible logic gates", International Journal of Scientific & Engineering Research, vol. 6, issue 6, **(2015)**, pp.327-332.
[11] M. P. Singh, B. Singh and A. Singh, "Performance Analysis of Low Power Decoders Using ReversibleComputing", International Journal of Research, vol. 2, issue 11, **(2015)**.
[12] Ankush and A. Singh Bhandari, "Design & Performance Analysis of Low Power Reversible Carry Skip Adder", IOSR Journal of VLSI and Signal Processing, vol. 6, issue 4, ver. II, **(2016)**, pp.33-39.
[13] S. Asri and M. Haghparast, "A Novel Nanometric Parity-Preserving Reversible Carry-Look Ahead Adder", IETE Journal of Research, DOI: 10.1080/03772063.2016.1205961.
[14] Ankush and A. Singh Bhandari, "Design & Performance Analysis of Low Power Reversible Residue Adder", International Journal of Hybrid Information Technology, vol. 9, issue 9, **(2016)**, pp.93-102.
[15] Palak, A. Singh Bhandari, "Design & Performance Analysis of 8-bit Low Power Parity Preserving Carry Look Ahead Adder", International Journal on Recent and Innovation Trends in Computing and Communication, vol. 5, issue 6, **(2017).**
[16] Ankush and Sonam, "An Improved Design of Low Power BCD Adder using Reversible Computing", International Journal of Advance Science & Technology, vol. 104, **(2017)**, pp.33-42
[17] Palak and A. Singh Bhandari, "Design & Performance Analysis of Low Power Ripple Carry Adder using Reversible Computing", International Journal in Applied Science and Production Management, vol. 3, issue 4, **(2017)**.
[18] Ankush and Sonam, "Efficient Design of Low Power Multiplier using MHNG Reversible Logic Gate", International Journal of Technical Research & Science, vol. 2, issue VIII, **(2017)**, pp.434-440

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