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An Improved Design of Low Power BCD Adder using Reversible Computing

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Abstract

In the field of quantum computation, the reversible logic and nanotechnology has gathered a lot of attention of researcher's in the recent years due to its low power dissipation quality. Quantum computing has been a guiding light for nanotechnology, optical information computing, low power CMOS design, DNA computing and Low power VLSI design. Arithmetic operations are the main component in any design of DSP or Microcontroller's, Multipliers and Divider circuits includes the additions and subtractions. Attempt is made in this paper to design an efficient BCD Adder circuit using reversible gates to minimize the quantum cost and power dissipation of the circuit. Synthesis and Simulation are verified using Xilinx 14.4 tool with Artix-7 kit.

Keywords*: Reversible logic, Combinational Circuit, BCD Adder, Quantum Cost, Power Measurement*

1. Introduction

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Part of the problem of energy dissipation is related to technological non-ideality of switches and materials. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer research, the amount of energy dissipated for every irrepressible bit Operation is at least KTln2 joules, where K = 1.3806505*10^23m^2kg^2K^1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Energy dissipation can be reduced or even eliminated if computation becomes Information--lossless Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history.

2. Reversible Logic

In the reversible logic, to prevent the loss of bit in logical operation, the number of inputs & outputs are made equal. Reversible gate is an n*n gate in which outputs can regenerate inputs, where n is number of inputs or outputs. To minimize the power dissipation, reversible logic gates are used instead of irreversible logic gates. In reversible

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gates, inputs & outputs are mapped one to one which will conserve energy as there will not be a loss of any bit.

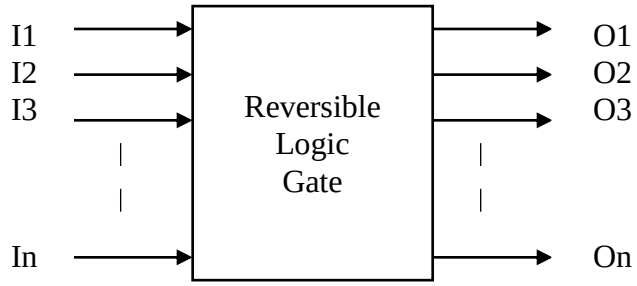


Figure 1. Block Diagram of Reversible Logic Gate

Features of reversible logic circuit:

I. Minimum number of reversible gates is used.
II. Minimum number of constant inputs is used.
III. Minimum number of garbage outputs should be there.
IV. The length of cascading gates is minimum.

3. Need of Reversible Computing

Reversible computing provide Reliable and low power design, high performance circuits synchronous with speed and processing power. Reversible circuits that conserve information, by incompetent bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. It again Improve computational efficiency this can be done by building circuits which reduce energy from state will save energy. Reversible computing will also lead to improvement in energy efficiency. It Increase portability of device to reduce element size to atomic size. It has incurred more hardware cost, but power cost and performance are dominant than hardware cost. Hence need of reversible computing cannot be ignored in computing era.

4. Parameters Related to Reversible Logic Gate

Following are the some useful parameters used while designing the Reversible Logic Circuits

4.1 Garbage Output

Garbage outputs are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations.

4.2 Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Calculating Quantum cost of reversible circuit is a significant one. Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and works are still going on in this area.

4.3 Gate Levels

This refers to the number of levels in the circuit which are required to realize the given logic functions. It should be minimum.

4.4 Hardware Complexity

Hardware Complexity refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit.

4.5 Gate Count

The number of reversible gates used to realize the function is basically known as Gate Count.

5. Types of Reversible Logic Gates

Following are the important reversible logic gates that are used in our proposed design

5.1 NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 2.

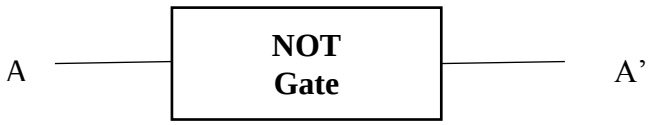


Figure 2. Block Diagram of NOT Gate

5.2 Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 3. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q= A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

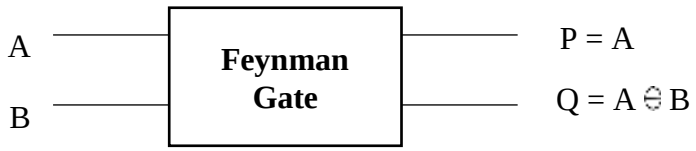


Figure 3. Block Diagram of Feynman Gate

5.3 MTSG Gate

Modified TSG (MTSG) gate is a 4×4 reversible gate with following input and output vectors, I = (A,B,C,D) and O =(P=A,Q=A⊕B,R = A ⊕ B ⊕ C and S = (A ⊕ B).C ⊕ (AB ⊕ D). This MTSG gate in Figure 4. It can be recycled to recognize a full adder by providing constant '0' at the input D. Quantum cost of MTSG gate is 6 which is lower than 13 of TSG gate

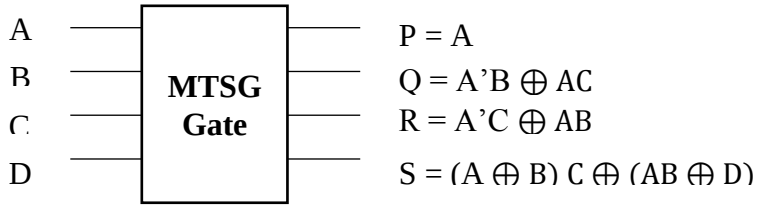


Figure 4. Block Diagram of MTSG Gate

5.4 NG Gate

It is a 3x3 gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). Its logic circuit diagram is shown in the figure 5. [10].

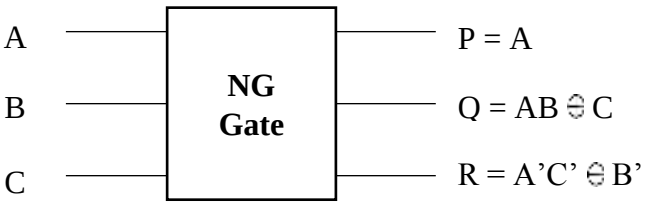
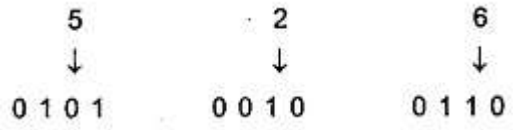


Figure 5. Block Diagram of NG Gate

6. Proposed Work

BCD Adder – The digital systems handles the decimal number in the form of binary coded decimal numbers (BCD). A BCD adder is a circuit that adds two BCD digits and produces a sum digit also in BCD. BCD numbers use 10 digits, 0 to 9 which are represented in the binary form 0 0 0 0 to 1 0 0 1**,** i.e. each BCD digit is represented as a 4-bit binary number. BCD numbers should not be greater than 9. When we write BCD number say 526, it can be represented as



BCD Code has applications in Decimal Number display Systems such as Counters and Digital Clocks. BCD Numbers can be added together using BCD Addition. BCD Addition is similar to normal Binary Addition except for the case when sum of two BCD digits exceeds 9 or a Carry is generated. When the Sum of two BCD numbers exceeds 9 or a Carry is generated a 6 is added to convert the invalid number into a valid number. The carry generated by adding a 6 to the invalid BDC digit is passed on to the next BCD digit.

A reversible BCD adder consists of three components: a 4-bit parallel adder, BCD adder overflow detection logic and BCD adder overflow correction logic. 4-bit full adder adds the BCD inputs and generates a binary sum, S (S3-S0).This output is checked for a value greater than '9' or for a carry out, by the 6- correction circuit which generates a '6-correction' bit, 'L' using Equation (1).

$$L = Cout + S3 (S1 + S2) \quad (1)$$

The general ideas of these designs are as follows: in the first 4- bit parallel adder, initial sum is produced by the binary addition of the two BCD numbers. In the combinational part, BCD overflow is detected. In the strict reversible sense, fan-out is restricted. Therefore, copying circuit is used. In the correction part, a 4-bit parallel adder is used to add the error correction value, i.e., in binary 0110, whenever overflow occurs. Otherwise, output produced by the first 4-bit parallel adder becomes the final output. However, there are scopes to improve the designs in terms of number of gates, garbage outputs, gate complexity and delay. We have proposed the design of reversible BCD adder using modified TSG gate, NG gate and Feynman Gates. The proposed design is shown in the figure 6.

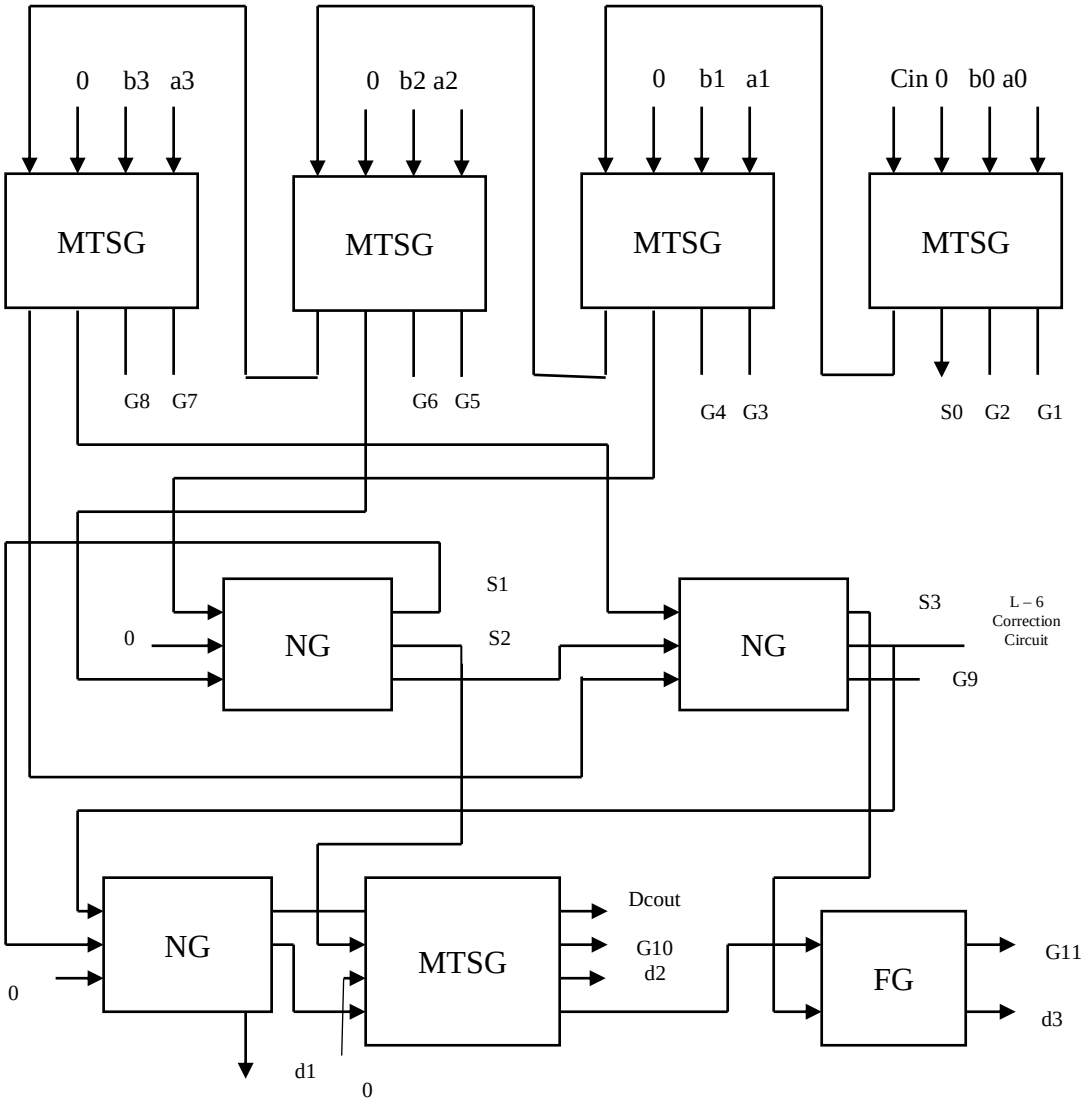


Figure 6. Proposed Design of Modified BCD Adder

The figure 6 shows the proposed design of BCD adder using MTSG, New gate and Feynman Gate. The 4*4 Modified TSG gate serves as full adder parallel circuit. The quantum cost of MTSG gate is 6 whereas the quantum cost of TSG gate is 9. The design strategy is chosen in such a way to reduce the most important factor of the reversible circuit quantum cost and power dissipation. The 3*3 NG gate serve as half adder. The BCD sum is indicated as d3-d0 carryout from the stage as 'Decimal Cout in Figure 6. This implementation uses 9 reversible gates and produces 11 garbage outputs.

Algorithm and Flow chart for reversible BCD adder:
Algorithm:
STEP 1: Clear previous outputs.
STEP 2: Read inputs.
STEP 3: Adding inputs.
STEP 4: Check the conditions, if condition is satisfied add 6 to sum otherwise store the result.
STEP 5: Exit.
Flow chart:
Figure 7 shows the flow chart for reversible BCD adder. First reset all previous carry and inputs. Then read the inputs A, B, Cin, and add the inputs. If sum is greater than 9 or carry generated from the carry bit add 6 to the sum otherwise sum is remain as it is.

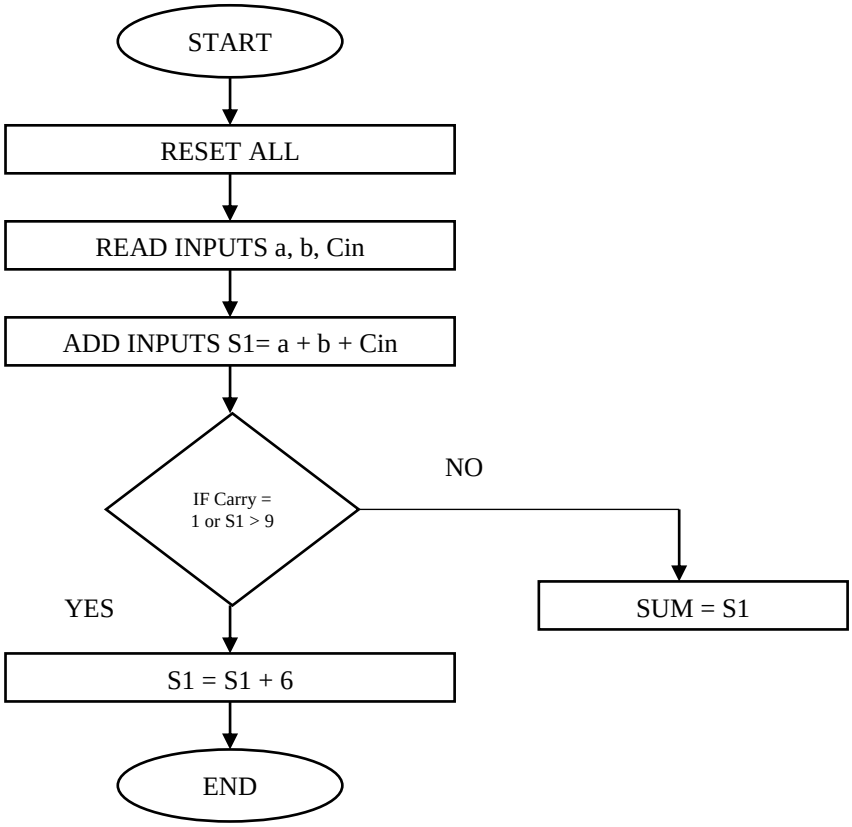


Figure 7. Flowchart of Reversible BCD Adder

7. Implementation & Results

Table 1. Comparison Table of Proposed Work with Existing Work

BCD Adder	Quantum Cost	Power Dissipation (W)
Proposed Design	46	3.441 W
Existing Design[5]	61	5.674 W

8. Simulation Methodology

The figure 8 shows the RTL schematic of top module for reversible BCD adder, it contains inputs a, b each of which contains 4 bits and Cin is the input carry. The D is the output which contains 4 bits and Cout is the output carry the figure 9 shows the RTL Schematic of Modified Binary adder with a0-a3, b0-b3, Cin as inputs, d0-d3 and Cout as outputs.

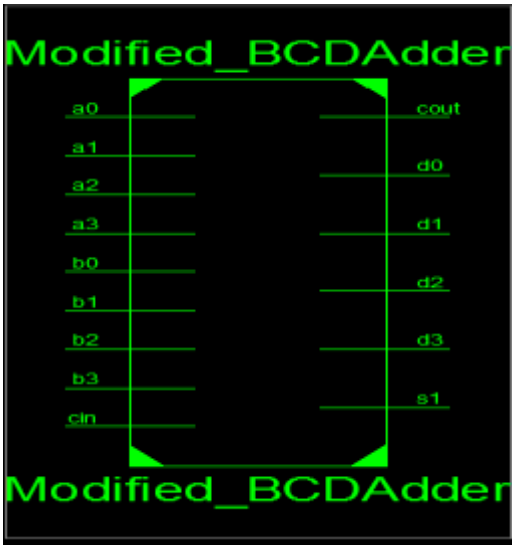


Figure 8. Block Diagram of Reversible BCD Adder

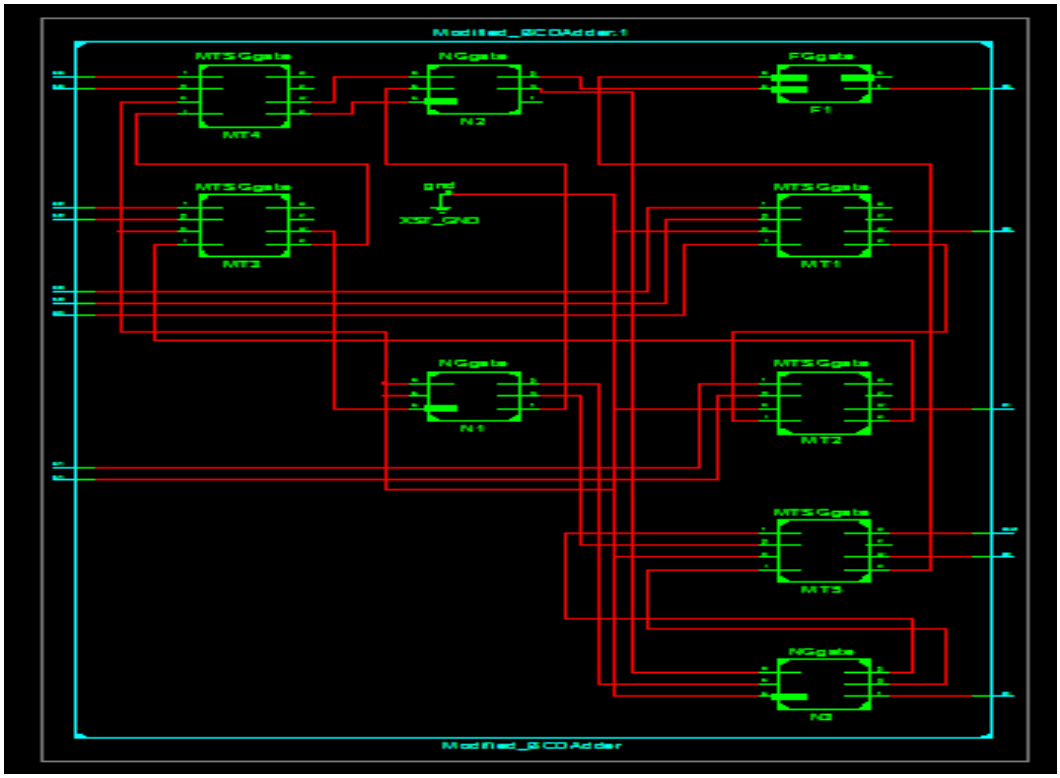


Figure 9. RTL View of Proposed Reversible BCD Adder

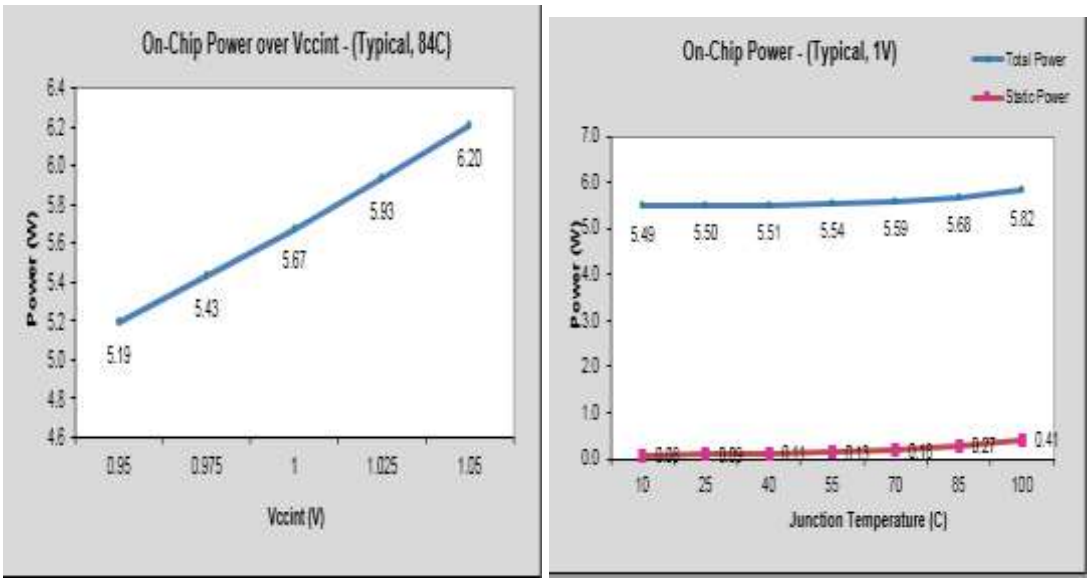


Figure 10. Power Dissipation Graph for Existing Reversible BCD Adder [5]

From Figure 10 the maximum dissipate power that is observed for BCD Adder using TSG gate, NG gate and Feynman gate and the maximum dissipate power obtained is 5.67W

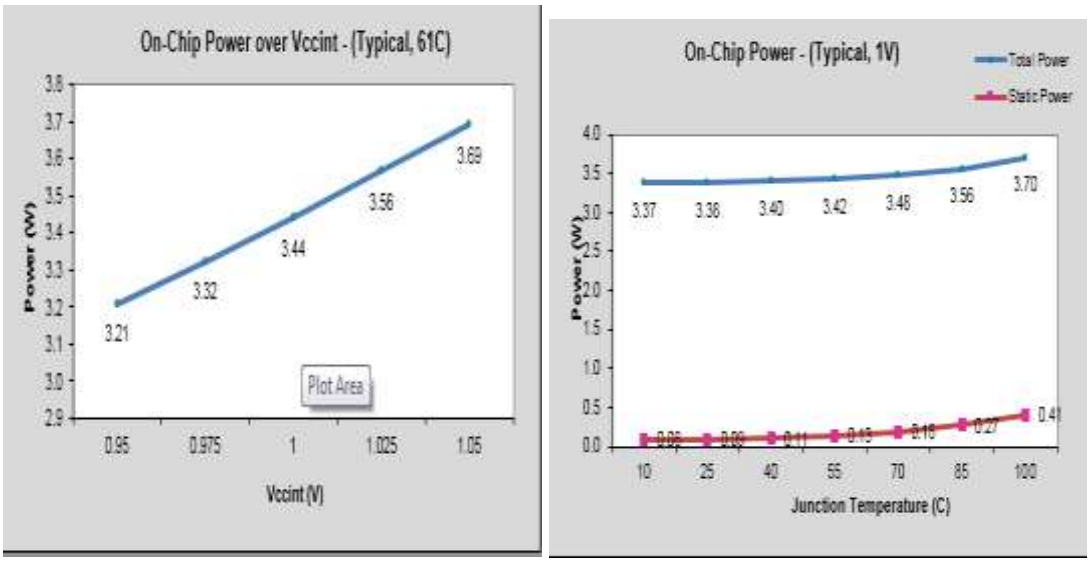


Figure 11. Power Dissipation Graph for Proposed Reversible BCD Adder

From Figure 11 the maximum dissipate power that is observed for Modified BCD Adder using modified MTSG gate, NG gate and Feynman gate and maximum dissipate power obtained is 3.44W

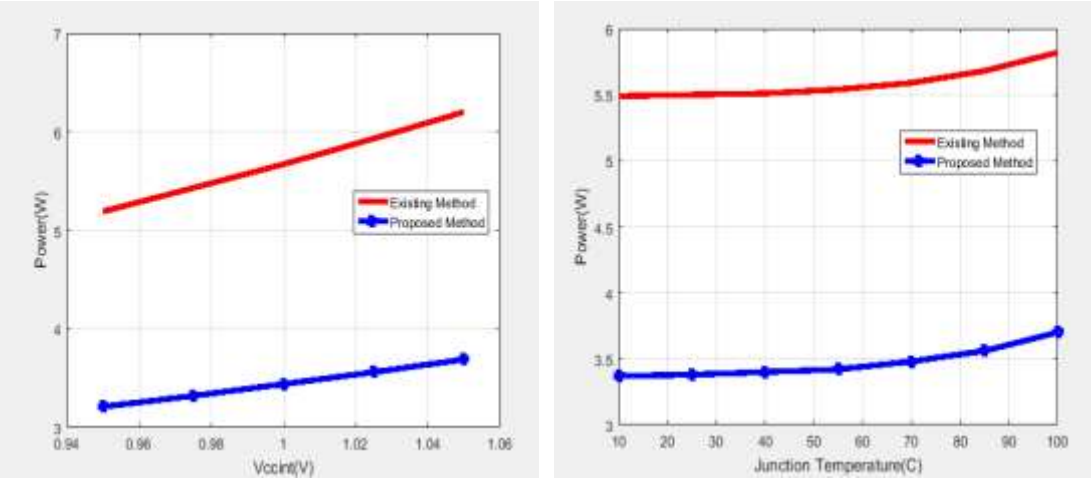


Figure 12. Comparative Results of Power Dissipation Graph for Proposed and Existing Reversible BCD Adder [5]

The comparative results of power dissipation graph for the proposed and existing reversible BCD adder shows that the proposed design dissipate very less power as compared to existing one. The graph between the Vcc & Power (figure 12) shows that the proposed design dissipate 3.441 Watt Power while the proposed design dissipate 5.674 Wattage of Power.

9. Conclusion

The reversible logic circuits are designed to minimize the power dissipation which ultimately increase the lifetime and speed of the circuit. The researchers are attracted towards reversible logic as it has enormous applications in the emerging technologies.

In this paper, we have presented efficient designs of reversible BCD adder primarily optimizing the parameters of Quantum Cost and Power Dissipation. In the existing system the quantum cost is 61 and power dissipation is 5.674 W but in our proposed work the quantum cost and the power dissipation parameters are reduced. We conclude that the use of the specific reversible gates for a particular combinational function can be very much beneficial in minimizing the power dissipation and quantum cost of the circuit. Further investigation into determining the delay & lesser area implementations can be done using logic synthesis methods.

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