Gate Engineering on the Analog Performance of DM-DG MOSFETs with High K Dielectrics

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Abstract

Considerable challenges are encountered when bulk CMOS devices are scaled into the sub-100 nm regime for higher integrated circuit (IC) density and performance. Due to their excellent scalability and better immunity to short channel effects, double-gate (DG) MOSFETs are being easily assessed for CMOS applications beyond the 70 nm of the SIA roadmap. For channel lengths below 100 nm, DG MOSFETs still show considerable threshold voltage roll off and to overcome this effect, different gate engineering techniques can be widely used. In this paper, we investigate the influence of gate engineering on the analog and RF performances of dual material double gate (DM-DG) MOSFETs for system-on-chip applications with high K dielectrics using a 2D device simulator. Equivalent oxide thickness (EOT) of gate oxide can be reduced by the usage of high K dielectric materials. The gate engineering technique used here is the dual metal gate technology. This novel structure shows better immunity to DIBL and improved analog performance like trans conductance generation factor, early voltage, output resistance.

Index Terms: *Carrier transport efficiency, dual material double gate (DM-DG), system-on-chip (SoC).*

1. Introduction

As technology scaling is pushing device dimensions into sub-0.1 μm regime, short channel effects and reliability issues have become areas of severe concern. Since conventional gate oxide thickness scaling gives rise to higher gate leakage, alternative approaches such as the use of gate engineering to alleviate these concerns will be a critical part of device design [1]. The continuous downscaling of CMOS technology has made it attractive for system-on-chip applications, where the analog circuits are realized with the digital systems in the same integrated circuit to reduce the cost and improve the performance [2], [3]. But conventional CMOS technology is facing greater challenges in terms of scaling due to reduced gate control, increased short-channel effects (SCEs) and high leakage currents [4]. The double-gate (DG) or multigate devices provide a better scalability option due to its excellent immunity to SCEs [5]–[7] Double gate (DG) MOSFETs have emerged as promising devices for nano-scale circuits due to their better scalability below 45 nm compared to bulk CMOS technology. Due to the presence of second gate, the effective gate control increases, reducing DIBL. Also the channel is very lightly doped or undoped and this results in reduced mobility

degradation. This technique also avoids random microscopic dopant fluctuations [15]. Gate engineering technique such as dual metal gate (DMG) MOSFET has been proposed in which the structure has two gates with different work functions [8-13].DMG MOSFET, in which two different materials having different work functions are merged together to form a single gate of a bulk MOSFET. In the DMG structure, the work function of the gate material (M1) close to source is chosen higher than the one close to drain end (M2) for n-channel MOSFETs. As a result, the electric field and electron velocity along the channel suddenly increases near the interface of the two gate materials which results in increased gate transport efficiency. This shows that the threshold voltage under gate material M1 is higher than that of under gate material M2.When the drain voltage exceeds the drain saturation voltage, the excess voltage is absorbed by gate metal M2 preventing the drain field from penetrating into the channel. This step potential is thus responsible for lower sub threshold leakage current, reduced DIBL effects and increased output resistance in DMG MOSFETS. This so called gate work-function engineering allows the DMG devices to have same threshold voltage for a reduced doping concentration in the channel region, resulting in better immunity to mobility degradation and hence higher transconductance [14]. Silicon dioxide has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current and device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to unwieldy power consumption and reduced device reliability [16]. Replacing the silicon dioxide gate dielectric with a high-K material allows increased gate capacitance without the leakage effects .An inverter is implemented with the device and its performance is analyzed.

2. Device structure and parameters

The schematic cross-sectional view of a dual material double gate MOSFETs implemented is shown in Fig.1a.The technology parameters and the supply voltages used for device simulations are according to International Technology Roadmap for Semiconductors (ITRS) 2005 edition for 100 nm gate length devices [13]. The oxide thickness is kept at 3 nm and a silicon film thickness of 20 nm. In the dual material double gate MOSFET, silicon film is kept practically undoped (10-15 cm 3), and the gate work function is fixed at 4.577 eV to obtain the threshold voltage of 0.3 V at a drain voltage of 0.1 V. As reported in [8] about the optimization of DMG technology, the work functions of metals M1 (molybdenum) and M2 (aluminum) are taken as 4.55 and 4.1 eV, respectively, with equal lengths of L1 and L2, and a threshold voltage of 0.3 V at a drain voltage of 0.1 V is obtained.

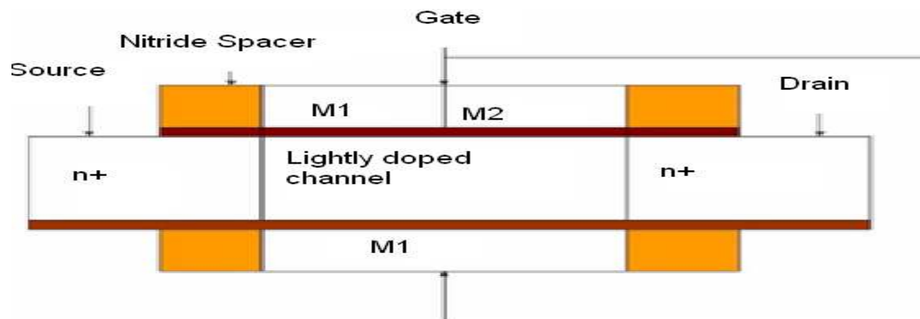

Figure 1. Cross-sectional views of the DM-DG MOSFET

3. Simulation results

A process simulator DIOS and device simulator DESSIS of integrated systems engineering technology computer aided design (ISE-TCAD) [12] are used for realization and analysis of all the devices used in this study. Simulations are performed for a wide range of proposed gate dielectric k values of 3.9, 7.8, 10, 15,25and 40.These dielectric constants correspond to SiO2, Si3N1, Al2O3, LaAlO3, HfO2 /ZrO2 and TiO2 repectively.In each simulation, the physical gate oxide thickness was proportionately scaled such that the electrical oxide thickness (EOT) remains the same.

3.1. Analog performance

The different analog performance parameters such as the transconductance gm, the transconductance generation factor gm/Id, early voltage and the output resistance Ro are studied in this section. The transconductance generation factor (TGF) or gm/Id ratio mentioned is viewed as the available gain per unit value of power dissipation. In a MOS transistor, gm/Id is maximum when in weak inversion and degrades severely with increasing drain current in the strong inversion regime. The transconductance generation factor with different gate to source voltage is shown in Fig. 2 for different high k dielectrics. It shows that transconductance generation factor is maximum for dielectric constant TiO2 and minimum for SiO2.

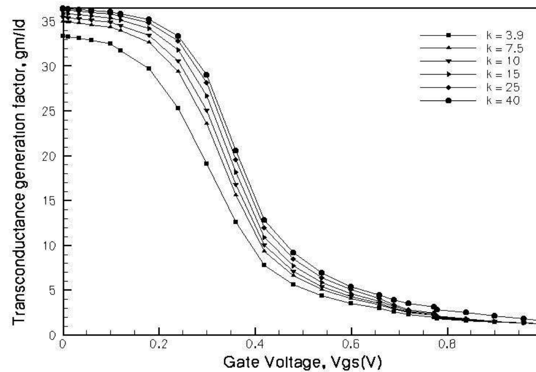

Figure 2. Plot showing the variation in transconductance generation factor with different gate to source voltage DM-DG MOSFET with increasing value of dielectric constant *k*

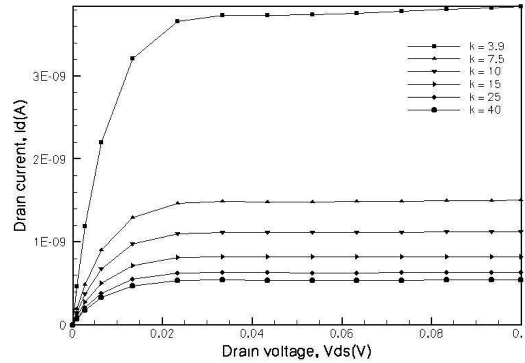

Figure 3. Plot showing the variation in drain current for different drain to source voltage DM-DG MOSFET with increasing value of dielectric constant *k*

The output resistance of a MOS transistor at any Vgs is evaluated as,

$$R_o = V_a / I_D$$

where Va and ID are early voltage and saturated drain current at that particular gate to source voltage. Such an improvement is due to the fact that the region of the channel under metal M2 provides a shielding effect such that the channel region under M1 is not affected by drain to source voltage variations. From Fig.8, it is clear that output resistance is maximum for dielectric constant TiO2 and minimum for SiO2.

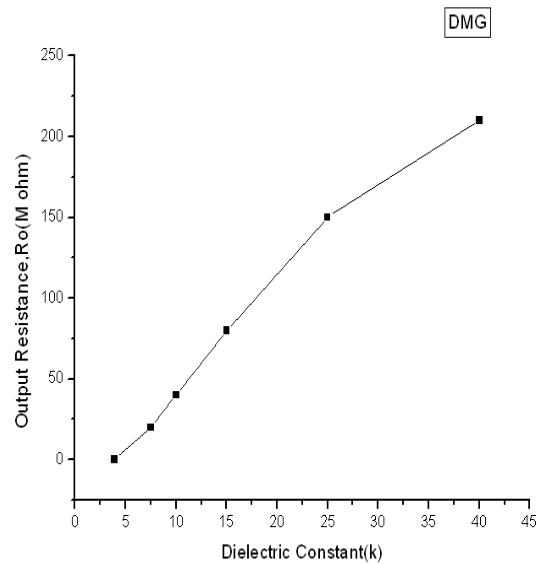

Fig. 4. Plot showing the variation in output resistance for different values of dielectric constant *k*

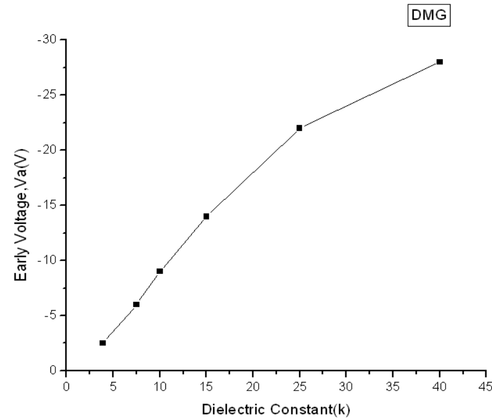

Figure 5. Plot showing the variation in early voltage for different values of dielectric constant *k*

From Fig.9, it is clear that early voltage is maximum for dielectric constant TiO2 and minimum for SiO2. And also if we use the same device in NAND circuits the power in VLSI circuits will be considerably reduce[19]

4. Conclusion

In this paper, we have clearly analyzed the influence of gate engineering on the analog performances such as transconductance generation factor, early voltage, output resistance of DM-DG MOSFETs. The performance of an inverter with different high k dielectrics is also illustrated using the DM-DG architecture. With the CMOS processing technology already into the 100-nm regime, fabricating DMG devices should not be complex in the near future. Thus, for thin-film silicon-on-insulator or DG MOS devices, the gate work function engineering such as the DMG technology is the most favorable technique for low-power sub threshold analog applications. The improvement is more prominent in the weak inversion regime thus making it more applicable for low power sub threshold analog performance.

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