Two Dimensional Analytical Modeling Of A Nanoscale Dual Material Gate MOSFETS

P. Suveetha Dhanaselvam
Lecturer,
ECE Dept, VCET
Madurai, India
suveethaj@rediffmail.com

Dr.N.B.Balamurugan
Assistant Professor
ECE Dept, TCE
Madurai, India
nbbalamurugan@tce.edu

P.Vanitha
Assistant Professor
ECE Dept, SIT
Madurai, India
vanitthh@yahoo.com

S. Theodore Chandra
PG Student,
ECE Dept, TCE
Madurai, India
theodore@tce.edu

Abstract

For more than 30 years, the IC industry has followed a steady path of constantly shrinking the device geometries and increasing chip size. A new gate structure called the dual material gate (DMG) MOSFET was proposed which eliminates the effects of reduction of chip size. A 2D analytical approach of DMG is proposed in this paper and the solution to the Poisson equation is obtained using parabolic expansion method. Using the boundary conditions, the surface potential and electric field potential distribution is obtained for different work function and channel lengths.

Keyword: *Dual material gate (DMG) MOSFET, parabolic expansion, surface potential, Electric field potential.*

1. Introduction

As MOSFET gate lengths are scaled down to sub-100 nm and gate oxide thickness to below 3 nm, short-channel effects (SCEs) such as: 1) increase in effective gate oxide thickness (EOT) due to polysilicon gate depletion; 2) threshold voltage change due to boron penetration from p+ polysilicon gate into the channel region; 3) degradation of device reliability due to gate leakage current (hot-electron effects); and 4) reduced gate controllability due to drain-induced barrier lowering (DIBL) become predominant. These SCEs [1] need to be eliminated or minimized for proper device operation. To eliminate polysilicon depletion width effects and polysilicon dopant penetration, polysilicon gates need to be replaced by metal gates. The dual-material-gate (DMG) FET was proposed and fabricated, taking two different metal gates as gate electrode [2]. DMG FET has two laterally contacting gate materials with different work functions to achieve threshold voltage modulation and improved carrier transport efficiency [3]. Shur [4] proposed a new field-effect transistor (FET) where the gate voltage swing (i.e., the difference between the gate voltage and the threshold voltage) is varied along the channel in such a way that the charge carriers are accelerated more rapidly and the average carrier velocity in the channel is increased. This can be achieved either by making the threshold voltage to be a function of position or by using a new device structure called split-gate FET (SG FET) If a more positive gate voltage is applied near the drain side than the electric field distribution along the channel is modified such that the electric field near the source becomes larger causing an increase in the gate transport efficiency. The realization of the SG FET structure is not a difficult task, but the

fringing capacitance between two metal gates increases as the separation between them is reduced and degrades the device performance [5]. However, this can be rectified if the separation between the two gates is made to be zero, but that leads to the conventional single gate structure. In 1999, Long *et al.* [5] proposed a new gate structure called the dual material gate (DMG)-MOSFET, as shown in Figure 1. Polishchuk *et al*. [6] proposed the fabrication of DMG-MOSFETs. In the DMG-MOSFET, the work function of metal gate 1 (M_1) is greater than metal gate 2 (M_2) i.e., and hence, threshold voltage which has the inherent advantage of improving the gate transport efficiency by modifying the electric field pattern and the surface potential profile along the channel. The step potential profile, due to different work functions of two metal gates, ensures reduction in the short-channel effects (SCEs) and screening of the channel region under M_1 from drain potential variations. Beyond saturation, M_2 absorbs any additional drain-source (D/S) voltage and hence the M_1 region is screened from the drain potential variations. In this structure, the peak electric field at the drain end is reduced, which ensures that the average electric field under the gate is increased. This enables an increased lifetime of the device, minimization of the ability of the localized charges to raise drain resistance and more control of gate over the conductance of the channel so as to increase the gate transport efficiency.

2. Analytical Model

A schematic structure of the n-type DMG MOSFET is shown in Figure 1. with $M_1$and M_2 of gate lengths L_1, and L_2, respectively. We have only studied n-type MOSFETs in our analysis, but it can be extended to p-type MOSFETs by minor modifications in the analysis. For analytical modeling, we have used V_s (substrate bias), N_A (substrate doping density), N_D (S/D doping density), and t_{ox} (thickness of dielectric ε_{ox})

. The 2-D Poisson's equation for potential distribution in the channel region is given

$$\frac{d^2\phi_i(x,y)}{dx^2}+\frac{d^2\phi_i(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{si}}, \quad 0<y<d \tag{1}$$

where i = 1, 2 corresponds to the region under M1 and M2, respectively, $\Phi_i(x, y)$ is the electrostatic potential in the channel, q is the electronic charge, d is the depletion width, and ε_{si} is the permittivity of silicon. The potential distribution in the channel is assumed to be a third-order polynomial function in the vertical direction. In the present analysis, the channel region has been divided into two parts, in which the potential under M_1 and M_2 can be represented as

$$\phi_1(x,y)=\phi_{S1}(x)+C_{11}(x)y+C_{21}(x)y^2+C_{31}(x)y^3 \text{ for } 0<x<L_1 \tag{2}$$

$$\phi_2(x,y)=\phi_{S2}(x)+C_{12}(x)y+C_{22}(x)y^2+C_{32}(x)y^3 \quad \text{for } L_1<x<L_1+L_2 \tag{3}$$

The Poisson's equation is solved separately [7-10] under the two regions M_1 and M_2 (because the metal work function is different for the two gates) using the boundary conditions (given in the Appendix A) (A_1)–(A_7) to obtain the coefficients C_{12} – C_{32}.

The 2-D potential distribution $\Phi_i(x, y)$ under M_1, and M_2 is found to be

$$\phi_1(x,y)=\phi_{S1}(x)-\left(\frac{V_{G1}'-\phi_{S1}(x)}{g_1}\right)y+\left(\frac{(3g_1+2d)}{g_1d^2}V_1(x)-\frac{3V_2}{d^2}\right)y^2$$
$$-\left(\frac{(2g_1+2d)}{g_1d^3}V_1(x)-\frac{2V_2}{d^3}\right)y^3 \qquad (4)$$

Where $V_1(x)=\left(V_{G1}'-\phi_{S1}(x)\right)$; $V_2=V_{G1}'+V_S$, $g_1=gt_{ox}$ (5)

Similarly, substituting the boundary conditions given in (A_1)-(A_7), finding out the constants and substituting in the equation (1).

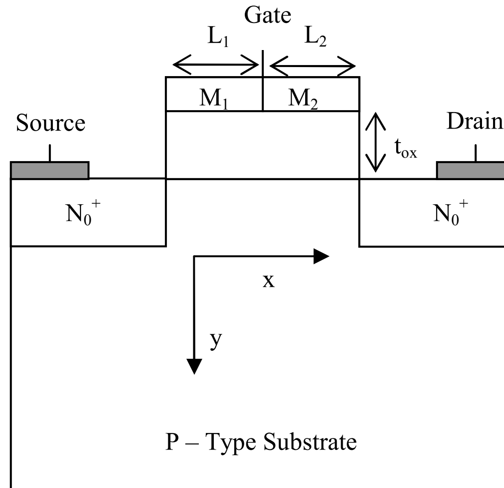

Figure 1. Schematic diagram of DMG MOSFET

Then substituting the expression of $\Phi_i(x, y)$ and $\Phi_i(x, y)$ in the equation (1), we obtain the solution as

$$\phi_{S1}(x)=V_{G1}'-\left(\frac{qN_A}{\varepsilon_{si}}+\frac{6\left(V_{G1}'+V_S\right)}{d^2}\right)\times c^2+e_1(x) \qquad (6)$$

$$\phi_{S2}(x)=V_{G2}'-\left(\frac{qN_A}{\varepsilon_{si}}+\frac{6\left(V_{G2}'+V_S\right)}{d^2}\right)\times c^2+e_2(x) \qquad (7)$$

Where, $$c = \sqrt{\frac{g t_{ox} d^2}{2\left(3 g t_{ox} + 2d\right)}}$$

and the expression for $e_1(x)$ and $e_2(x)$ are introduced to simplify calculations given in the Appendix B.

The concept of DIBL effect can be illustrated by the channel surface potential. Since the subthreshold leakage current often occurs at the position of minimum surface potential, therefore, the influence of DIBL on the subthreshold behavior of the device can be monitored by the minimum surface potential. The surface electric field component along the channel (i.e., in the *x*-direction) is an important parameter because electron velocity along the channel can be determined from it. The position of minimum surface potential lies under M1 and can be evaluated by solving the differential equation of $\Phi_{S1}(x)$ and equating to zero. The steps involved in solving this equation and finding out the value of x_{min} and minimum surface potential is given in Appendix B.

As the electron transport velocity through the channel is related to the electric field pattern along the channel, the electric field component, in the x direction under M_1 is obtained as

$$E_1(x) = \frac{d\phi_1(x,y)}{dx}\Big|_{y=0} = \frac{d\phi_{S1}(x)}{dx} = \frac{e_{10}\left(\frac{-1}{c}\right)\cosh\left(\frac{L_1 - x}{c}\right) + e_1 L_1\left(\frac{1}{c}\right)\cosh\left(\frac{x}{c}\right)}{\sinh\left(\frac{L_1}{c}\right)} \quad (8)$$

Similarly, the electric field component in the x direction under M_2 is given by the expression

$$E_2(x) = \frac{d\phi_2(x,y)}{dx}\Big|_{y=0} = \frac{d\phi_{S2}(x)}{dx} = \frac{e_{20}\left(\frac{-1}{c}\right)\cosh\left(\frac{L-x}{c}\right) + e_2 L_2\left(\frac{1}{c}\right)\cosh\left(\frac{x-L_1}{c}\right)}{\sinh\left(\frac{L_2}{c}\right)} \quad (9)$$

3. Results And Discussion

Figure 2 shows the calculated surface potential profile for different channel length of the DMG structure along with the calculated potential profile. It shows the variation of surface potential along the normalized channel position for DMG-MOSFET for different gate lengths. It is evident from that there is a step-change of potential along the channel at the interface of M_1 and M_2. As the zero-field point or the point of maximum barrier shift toward the source, the gate loses its control over the channel and device reaches punchthrough.

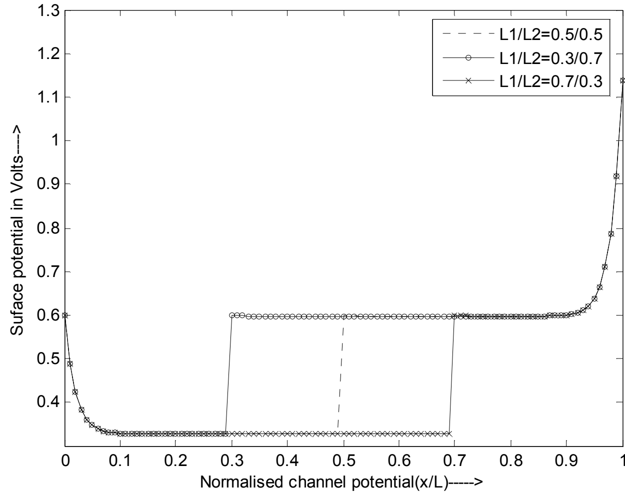

Figure 2. Surface potential profiles of DMG MOSFETs for different combination of gate lengths L_1 and L_2

Figure 3 shows the calculated values of the electric field along the channel length at the drain end for the DMG SOI MOSFET for the channel length. Because the continuity in the surface potential of the DMG structure, the peak electric field at the drain is reduced substantially.

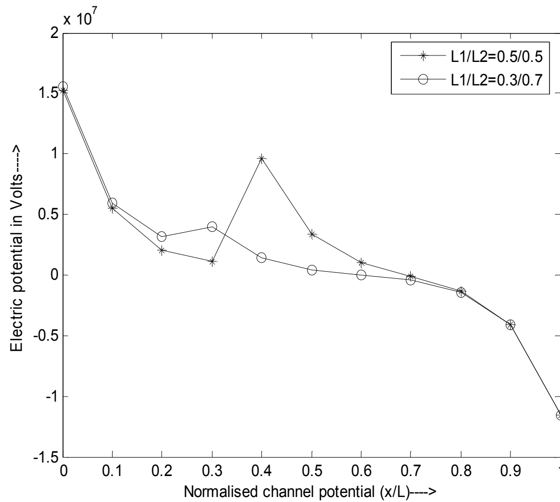

Figure 3. Longitudinal electric field along the channel toward the drain end obtained from the analytical model of DMG MOSFETs for different gate lengths L_1 and L_2

4. Conclusion

The DMG-MOSFET structure has been analyzed and its performance improvement over different values are discussed. From the presented results, it can be concluded that that

the DMG structure has wide range of benefits to the FET performance. The step-function profile in the surface potential exhibits improvement in screening of the drain potential variation, and reduced SCEs. The ratio of the length of the two metal gates can be optimized with asymmetrical doping profile along the channel for future generation of hot electron resistant devices with sub-100-nm gate lengths. The results unambiguously establish that the incorporation of DMG structure in a MOSFET leads to subdued short-channel effects due to a step-function in the surface potential profile. The shift in the surface potential minima position is negligible with increasing drain biases. The electric field in the channel at the drain end is reduced leading to reduced hot-carrier effect. The results clearly demonstrate the excellent immunity against SCE offered by the DMG structure by decreasing channel length.

APPENDIX A

BOUNDARY CONDITIONS USED TO DEVELOP THE ANALYTICAL MODEL

1) Surface potential is continuous at the interface ($x = L_1$ and $x = L_1 + L_2$) of two dissimilar metals at the gate oxide/Si interface ($y = 0$), i.e.,

$$\phi_1(L_1, 0) = \phi_2(L_1, 0) \qquad (A_1)$$

2) Electric flux is continuous at the interface ($x = L_1$ and $x = L_1 + L_2$) of two dissimilar metals at the gate oxide/Si interface ($y = 0$), i.e.,

$$\frac{d\phi_1(x,y)}{dx} = \frac{d\phi_2(x,y)}{dx} \quad \text{at } x = L_1 \qquad (A_2)$$

3) Electric field at depletion edge is equal to zero where the effective depletion width is d, i.e.,

$$\frac{d\phi_1(x,y)}{dx} = \left(\frac{V_{G1}' - \phi_{S1}(x)}{gt_{ox}}\right) \qquad (A_3)$$

$$\frac{d\phi_2(x,y)}{dy} = \left(\frac{V_{G2}' - \phi_{S1}(x)}{gt_{ox}}\right) \qquad (A_4)$$

4) The potential at the substrate is $-V_{SUB}$ (V_{SUB} is applied substrate-to-source voltage) at depletion edge, i.e.,

$$\phi_1(x, d) = \phi_2(x, d) = -V_S \qquad (A_5)$$

5) At the source end, we have

$$\phi_1(0,0) = \phi_{S1}(0) = V_{bi} \qquad (A_6)$$

6) At the drain end, we have

$$\phi_1(L,0)=\phi_{S2}(L)=V_{bi}+V_{DS} \quad (A_7)$$

Where V_{bi} is the built-in-potential and V_{DS} is the drain to-source voltage.

APPENDIX B

VARIOUS COEFFICIENTS OF SURFACE POTENTIAL IN THE TWO DIFFERENT REGIONS

Equation (6) and (7) can be written as:

$$e_1(x)=\frac{e_{10}\sinh\left(\frac{L_1-x}{c}\right)+e_1L_1\sinh\left(\frac{x}{c}\right)}{\sinh\left(\frac{L_1}{c}\right)} \quad (B_1)$$

$$e_2(x)=\frac{e_{20}\sinh\left(\frac{L}{c}\right)+e_2L_2\sinh\left(\frac{x-L_1}{c}\right)}{\sinh\left(\frac{L_2}{c}\right)} \quad (B_2)$$

Where the constants of the equation are found using the following boundary conditions

$$e_1(0)=V_{BI}-V_{G1}'+\left(\frac{qN_A}{\varepsilon_{si}}+\frac{6\left(V_{G1}'+V_S\right)}{d^2}\right)c^2 \quad (B_3)$$

$$e_2(L_1+L_2)=e_{2L2}=V_{BI}+V_{DS}-V_{G2}'+\left(\frac{qN_A}{\varepsilon_{si}}+\frac{6\left(V_{G2}'+V_S\right)}{d^2}\right)c^2 \quad (B_4)$$

Using the boundary conditions given in Appendix A, we can find the following parameters

$$e_{20}=\frac{k_3+k_2m_1}{k_1+k_2} \quad (B_5)$$

$$e_{1L1}=e_{20}-m_1 \quad (B_6)$$

Where the constants are given as:

$$k_1=\frac{1}{c}\sinh\left(\frac{L_1}{c}\right)\cosh\left(\frac{L_2}{c}\right) \quad (B_7)$$

$$k_2=\frac{1}{c}\sinh\left(\frac{L_2}{c}\right)\cosh\left(\frac{L_1}{c}\right) \quad (B_8)$$

$$k_3 = e_{10}\left(\frac{1}{c}\sinh\left(\frac{L_2}{c}\right)\right) + e_{2L2}\left(\frac{1}{c}\sinh\left(\frac{L_1}{c}\right)\right)\cosh\left(\frac{L_2}{c}\right) \quad (B_9)$$

$$m_1 = \left(1 - 6\left(\frac{c}{d}\right)^2\right)\left(V_{FB2} - V_{FB1}\right) \quad (B_{10})$$

The minimum surface potential is given as

$$\phi_{S1}\left(x_{\min}\right) \approx V_{G1}{}' - \left(\frac{qN_A}{\varepsilon_{si}} + \frac{6\left(V_{G1}{}' + V_S\right)}{d^2}\right)c^2 + 2\sqrt{e_{10}e_{1L1}}\exp\left(\frac{L_1}{2c}\right) \quad B_{11})$$

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Authors

P.Suveetha Dhanaselvam was born on 29-12-1979.She received her B.E degree in Electronics and Communication Engineering from St.Peter's Engg. College,Chennai and her M.E degree in Applied Electronics in Sathyabama Institute of Technology, Chennai, Tamilnadu, India. She is currently doing research work in nanoelectronics. She has teaching experience of about 6 yrs.Initially she worked as a Lecturer in Tagore Engg.College, Chennai. At present , she is working as a Lecturer in Velammal College of Engineering and Technology, Madurai, Tamilnadu, India. She has published 5 papers in National and International Conferences.Her areas of interest include modeling and simulation of multigate SOI MOSFETs
Email: suveethaj@rediffmail.com

Dr. N. B. Balamurugan received his B.E and M.E degrees, both in electronics and communication engineering from the Thiagarajar College of Engineering (TCE), Tamilnadu, India. He has obtained his Ph.D degree in nanoelectronics at Anna University, India. From 1998 to 2004, he worked as a lecturer in R.V.S.college of engineering and technology, Tamilnadu, India. He is currently as an Assistant Professor in Thiagarajar College of Engineering (TCE), Tamilnadu, India. He has published more than 20 papers in both International and National conferences.His research interests include modeling and simulation of novel structures on SOI MOSFETs. Email:nbbalamurugan@tce.edu

P.Vanitha received her B.E degree in Electronics and Communication Engineering from R.V.S. college of engineering and technology, Dindigul and her M.E degree in Applied Electronics in Sathyabama Institute of Technology, Chennai.She is doing research in the area of nanodevices.She has a teaching experience of about 12 years .She is currently working as an Assistant Professor in Sethu Institute of Technology, Madurai, Tamilnadu, India . She has published 5 papers in various National and International Conferences. Her areas of interest include modeling and simulation of nanoscale MOSFETs. Email:vanitthh@yahoo.com

Theodore Chandra was born in Tamilnadu, India, on September 13, 1981. He received his B.E. degree in Electronics and Communication Engineering from Francis Xavier Engineering College, Tirrunelveli, Anna University, Chennai, in 2008. He is currently pursuing his M.E. degree in Communication Systems at Thiagarajar College of Engineering, Madurai, where he is involved in 2-D analytical modeling of short channel effects in DMG MOSFET structure. His research interest includes analysis and modeling of Dual Material Gate MOSFET. He has published 2 papers in international and national conferences.
Email: theodorechandra@in.com