A Novel Integrated Photonic Band Gap Substrate With Wideband Suppression Of High Frequency Switching Noise And Its Radiated EMI On High Speed Devices

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Abstract

Simultaneous switching noise (SSN) compromises the integrity of the power distribution structure on multilayer printed circuit boards (PCB). In this paper a novel photonic crystal power/ground layer (PCPL) is proposed to efficiently suppress the power/ground bounce noise (P/GBN) or simultaneously switching noise (SSN) in high-speed digital circuits. The PCPL is designed by periodically embedding high dielectric-constant rods into the substrate between the power and ground planes. The PCPL can efficiently suppress the high frequency noise and its radiated EMI generated be the SSN (over 60 dB) with broad stop band bandwidth (totally over 4 GHz below the 10-GHz range, and in the time domain, the P/GBN can be significantly reduced over 90%. The PCPL not only performs good power integrity, but also keeps good signal quality with significant improvement on eye patterns for high-speed signals with via transitions. In addition, the proposed designs perform low radiation of electromagnetic interference caused by the SSN within the stop bands. These extinctive behaviors both in signal integrity and electromagnetic compatibility are demonstrated numerically and experimentally.

Key-Words:- *Electromagnetic band gap (EBG), electromagnetic interference (EMI), high-speed digital circuits, photonic crystal, Power/Ground Bounce Noise (P/GBN), Power Integrity (PI), Signal Integrity (SI), simultaneously switching noises (SSNs).*

1. Introduction

In the good olden days of 10MHz clock frequency, a device would output a signal with a rise time of roughly 10 nsec and a clock frequency of 10 MHz. But clock frequencies have increased and rise times of signals have decreased. For most electronic products, signal-integrity effects begin to be important at clock frequencies above of about 100 MHz or rise times shorter than about 1 nsec. This is sometimes called the high-frequency or high-speed regime.Many modern packaging structures support mixed signal systems, where both the analog and digital circuits exist together with common power/ground plane in the PCB's. With the increase in the operating frequency range for various applications, the PCBs with both the sensitive RF/analog circuits and high speed digital circuits operate in RF frequencies. The digital circuits have fast switching time (rise time), high clock frequency and low voltage level. The operating frequency range of these High Speed Printed Circuit Boards with RF/analog circuits and high speed digital circuits will be high in the range of GHz. SI refers, in its broadest sense, to all the problems that arise in high-speed products at high frequencies

due to the interconnects. It is about how the electrical properties of the interconnects, interacting with the digital signal's voltage and current waveforms, can affect performance. Lot of signal-integrity noise problems are there such as ringing, ground bounce or switching noise, reflections, near-end cross talk, non-monotonicity, power bounce, attenuation and capacitive loading. All of these relate to the electrical properties of the interconnects and how the electrical properties affect the waveforms of the digital signals.

With clock frequencies increasing, the radiated emissions level will inevitably increase as well. Every source of signal-integrity problem mentioned above will be a source of EMI. The two most common sources of EMI are (1) the conversion of some differential signal into a common signal, which eventually gets out on an external-twisted pair cable, and (2) ground bounce on a circuit board generating common currents on external single-ended shielded cables. Additional noise can come from internally generated radiation leaking out of the enclosure. Due to inductive or capacitive coupling between the interconnects or traces, cross talk will occur. When the signal goes through a connector and when the return paths for more than one signal path are shared by one of the pins rather than by a plane, the inductively coupled noise increases much more than the capacitively coupled noise. In this regime, where inductively coupled noise dominates, we refer to the cross talk as switching noise, delta I noise, di/dt noise, ground bounce, simultaneous switching noise (SSN), or simultaneous switching output (SSO) noise.

1.1 Simultaneous Switching Noise.

As digital devices become faster, their switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents which are generated when multiple outputs of a device switch simultaneously from logic high to logic low can cause a board-level phenomenon called as Ground Bounce Noise (GBN) or Simultaneous Switching Noise (SSN). Simultaneous switching Noise is an inductive noise and it depends on the geometry of the system and current paths. SSN can be described by

$$V_{Noise} = NL_{eq}\frac{di}{dt} \quad \text{------ (1)}$$

where V_{Noise} is the Ground Bounce or Simultaneous Switching Noise, N is the number of output drivers switching simultaneously, L_{eq} is the equivalent inductance. Simultaneous Switching Noise on the power/ground plane is becoming one of the major concerns for the high speed digital computer systems with fast rise time, high clock frequency and low voltage level because it will cause breakdown of the sensitive RF circuits and in the worst case, bursting of the analog circuits. So this Simultaneous Switching Noise (SSN) has to be reduced Adding decoupling capacitors between power and ground planes is a typical way to eliminate the SSN and EMI, but they are not effective above several megahertz due to the effective series inductance of the capacitors. The embedded capacitance with a very thin dielectric layer between the power and ground planes are another solution to suppress the SSN[4]. However, the electromagnetic waves still propagate between the planes with resonance at specific frequencies. Recently, several electromagnetic band gap (EBG) structures employing either the high-impedance surface (HIS) concept [5]–[7] or the long-period coplanar (LPC) EBG design [8], [9] on the power or ground planes are proposed to eliminate the P/GBN in high-speed circuits. The basic idea of these EBG structure is periodically cascading the designed unit cell with specific *L* and *C* characteristics to form a band stop filter. These structures are realized on the power or ground planes with several etched slits on the metals. These EBG power/ground planes design behaves like broadband

SSN isolation and EMI elimination, but the SI issue could arise for the signal traces referring to the imperfect ground or power planes with slits [10]. This paper proposes a photonic crystal power/ground layer (PCPL) to eliminate the SSN and corresponding radiated emission without etching the power or ground metal planes.

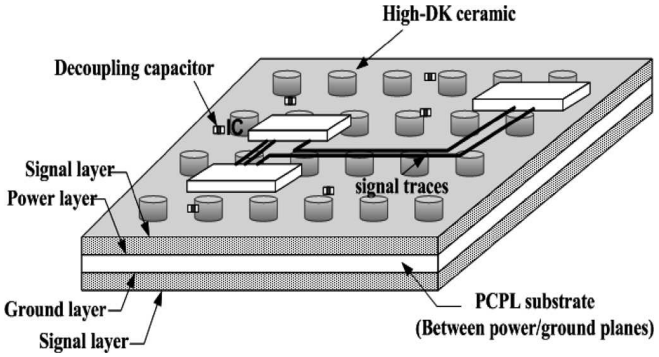

Fig. 1.PCPL concept in a typical four layer high-speed PCB circuits.

The main idea of the PCPL is periodically embedding the relatively high dielectric-constant material (rods) into the original isolation layer between the solid power and ground planes. The two dimensional (2D) photonic crystal layer with a periodic dielectric Contrast will form a stop band and can be used to suppress the resonant modes excited by the SSN inside the power/ground parallel plat e. By suitably choosing the pitch and dimension of the embedded rods, the stop band of the PCPL can be designed at frequencies below 10GHz, where the P/GBN is dominantly distributed in high-speed circuits [5] with the rejection bandwidth totally above 4 GHz. Based on the 2-D finite-difference time-domain (FDTD) approach, the design diagram for the frequency range and the bandwidth of the stop band for the PCPL is calculated. The advantages of the proposed PCPL are broad stop band for SSN with a very low filling ratio of the high dielectric- constant rods, good SI with continuous power and ground planes, and an easy fabrication process compatible with standard package [or printed circuit board (PCB)] substrate manufacturing. This idea was recently proven for the capability of noise suppression in a chip package substrate with small area, but the performance is not very satisfied. This study not only extends the idea to the PCB-like substrate (larger area) with significantly improved noise suppression performance, but also provides a complete theoretical and experimental investigation of the PCPL behavior both in the time and frequency domains, the impact of the PCPL for SI and electromagnetic compatibility (EMC), and the design strategies for the proposed structure. Photonic crystal structures have been widely used in the fiber communication and microwave circuit design, but the application in the SSN suppression for high-speed circuits, to the best of our knowledge, has not been seen in the previous literature.

2. PCPL MODEL AND DESIGN BY 2-D FDTD METHOD

2.1 PCPL Concept

Fig. 1 shows a PCPL concept in typical four-layer high-speed PCB circuits. Top and bottom layers are for routing signal traces between the circuit components such as integrated circuits and passive elements. The inner two layers, i.e., the second and third layer, are

typically for power and ground planes. In typical packages, the substrate thickness is very thin and it can be assumed that only TM modes propagate between the parallel-plate cavity formed by the power and ground planes. The PCPL concept is periodically embedding high dielectric-constant rods between the power and ground planes, as shown in Fig. 1, to eliminate the propagation of the TM modes. From the SI and EMI point-of-view, keeping the reference planes continuous is important to have a good return path for the high speed signals. Therefore, consistent with the layout strategy for the high-speed circuit package, there are no additional etching slots or partitioning on the metal power or ground planes in our proposed design. The P/GBN and their corresponding EMI are omni-directionally and efficiently suppressed by the EBG of the PCPLs.

2.2. PCPL Design and Fabrication

Figure-2 shows two PCPL designs with square lattice (SL) of 40(8 by5) embedded rods and triangular lattice (TL) of 39 embedded rods on a two-layer Rogers/Duroid 5870 substrate. The dimension of the substrate for the SL-PCPL and TL-PCPL is 62.5mm × 100mm and 60mm × 60mm, respectively, with 0.8 thickness. The dielectric constant of the substrate in ε_{r0} =2.33.The radius of the circular rod and the pitch between the rods are denoted as *r* and *a*, respectively. The *r/a* is designed as 0.16 and 0.12, respectively, for the SL-PCPL and TL-PCPL. The high dielectric-constant rod with 2mm radius and 00.8mm height is fabricated with the mixing of $BaCO_3$ and TiO_2 under typical ceramic fabrication process. The dielectric constant ε_{r1} of the rods is about 102. The top and bottom faces of the circular rods are coated with silver metal. The PCPL is simply fabricated by drilling the 2mm-radius holes on the substrate at designed positions and embedding the circular rods into the holes. Two measurement ports, port1 and port2, are located at (25mm, 12.5mm) and (47mm, 23.5mm), respectively, for the SL-PCPL and (50mm, 15mm) and (42.5mm, 40mm), respectively for the TL-PCPL. It is noted that the filling ratio A_r, defined as the total area of all the embedded rods into the area of the substrate, is only about 8% and 13% for the SL-PCPL and TL-PCPL, respectively. The structure is modeled using ANSOFT HFSS .

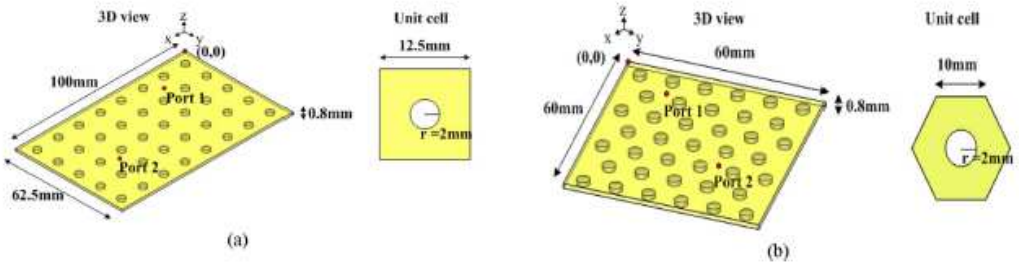

Fig. 2. Schematic diagram of proposed test boards. (a) SL PCPL board. (b) TL PCPL board.

3. PI/SI PERFORMANCE

3.1. PI Performance

1) Frequency Domain: We first see the band stop behavior for eliminating the P/GBN in the frequency domain. Fig. 4 the simulated S_{21} for the SL PCPL and TL PCPL, respectively. The behaviors of the reference board without embedding the high dielectric-constant rods are also

included in these two figures for comparison. Ansoft's High Frequency Structure Simulator (HFSS) is used to simulate the S-parameters for all the power/ground-plane structures. Good agreement between measurement and modeling is obtained. A slight discrepancy at frequencies above 5 GHz is seen for both PCPL boards. The reasons could be that the fabrication accuracy for drilling holes and their alignment is not good enough for the prototype boards. As shown in Fig. 4(a) and (b), there are two stop bands for both the SL PCPL and TL PCPL below 8 GHz. The bandwidth of the SL PCPL for the first stop band is second band. The bandwidth for the TL PCPL is approximately 2.6 GHz (from 2.8 to 5.4 GHz) and approximately 2.6 GHz (from 2.6 to 5.2 GHz) and approximately 1.3 GHz (from 5.8 to 7.1 GHz) for the 1.6 GHz (from 6 to 7.6 GHz) for the first and second stop bands, respectively. The bandwidth is defined by the insertion loss less than 30 dB. There are other stop bands above 8 GHz, but it is not discussed in this study because we are interested in the P/GPN dominantly distributed below 10 GHz. For the SL PCPL, it is seen the power plane resonance noise on the reference board at 2.9, 3.2, 3.9, and 5.0 GHz are efficiently reduced over 70 dB by the SL PCPL. The P/GBN is reduced over 60 dB on average within the first stop band, which is an excellent performance for suppressing the SSN coupling. For the second stop band, the noise peak at 6.2 GHz is reduced approximately 35 dB, and on average, there is over 25-dB noise elimination capability. For the TL PCPL, it is found the power plane noise on the reference board at 3.2, 3.7, and 5.0 GHz are efficiently eliminated over 70 dB. The P/GBN is reduced over 60 dB on average within the first stop band, which is similar to the performance of the SL PCPL. For the second stop band, the noise peak at 6.2 GHz is reduced approximately 50 dB, and on average, there is over 40-dB noise suppression. It is also found that TL PCPL has almost the same bandwidth for the first stop band, but significantly larger bandwidth for the second band, which is similar to the band structure prediction shown in Fig.3. It is noted that there are additional resonant peaks, which are not seen in the reference boards, which appear below the first stop band (from dc to approximately 2.8 GHz) for both PCPL boards. However, as shown in Fig. 3(a) and (b), these peaks would not worsen the P/GBN coupling because the effective dielectric constants of the PCPL are increased significantly. The effective dielectric constant is defined as

$$\varepsilon_{eff} = A_r\varepsilon_{r1} + (1-A_r)\,\varepsilon_{r0} \quad \text{----------} \quad (1)$$

which is 10.348 for the SL PCPL and 15.899 for the TL PCPL. The equivalent parallel-plate capacitance for the SL PCPL and TL PCPL is pF and pF, respectively. The insertion loss of the shunt capacitor is also plotted in Fig. 3(a) and (b), and is quite consistent with both the measured and simulated results at low frequency below the first resonant peak. It can be clearly seen that the increase of the effective dielectric constant not only significantly reduces the power noise coupling between the two ports at frequency below 500 MHz, but also decreases the coupling strength at those resonant peaks below approximately 2.8 GHz

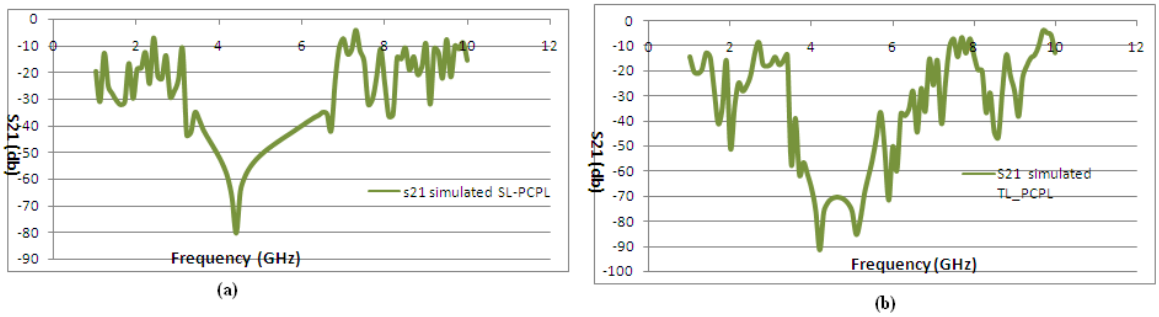

Fig. 3. Comparison of S12 obtained by HFSS and measurement for: (a) SL PCPL board (b) TL-PCPL

3.2. SI Performance

Fig.1 shows a typical high-speed signal trace routing on a four-layer PCB two via-transitions between the top and bottom layers. The PCPL is designed in the inner two layers. Since the power and ground metal planes are perfect (or continuous), the influence of the PCPL on the signal quality could only result from the via-transitions .It is well known that through-hole via transition will excite the noise between the power and ground planes and degrades the SI. The SI performance of the proposed PCPL is discussed here. The input signal is 10 Gb p/s with 500-mV amplitude and 35-ps edge rate .The traces quality. It is seen that for the TL PCPL, 292mV and 85ps, and for the reference board, mV and 72ps .Compared with the reference board, the MEO and MEW is significantly improved approximately 19% and 18% for the TL PCPL. The SL PCPL has a similar SI improvement capability as the TL PCPL does and is not shown here.

4. DESIGN DIAGRAM

The bandgap map for the SL PCPL and TL PCPL, is designed by the 2-D FDTD method. The dependence of the normalized stopband distributions on the normalized radius (r/a) of the high dielectric-constant rods for the first three bands are presented, where is the speed of light in free space. The first stopband for both PCPL appear for small radius at approximately r/a=.03 with narrow bandwidth. The bandwidth gradually increases with center frequency decreased as r/a is increased. It is found that there is maximum bandwidth of for the SL PCPL and for the TL PCPL, as r/a is designed between 0.08–0.1.

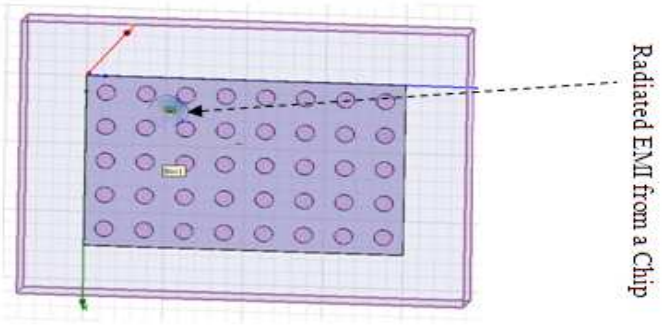

Fig. 4. E-Field Overlay pattern in the PCPL Board.

The bandwidth of the first stopband decreases gradually with the center frequency decreased as r/a is increased from 0.1 for both PCPL. The bands will disappear as r/a is larger than approximately 0.45, where the substrate is almost filled with high dielectric-const ant rods. Similar phenomena are seen for the second and third stopbands. Figure – 4 shows the E-field being attenuated in between the photonic band gaps. For the application of suppressing the P/GBN in this study, we need the broad stopband at a low-frequency range below 10 GHz. Therefore, there is design tradeoff between the bandwidth and center frequency for the PCPL structure. As described in Sections III and IV, we design the SL PCPL with r/a=.16 and the TL PCPL with r/a=.2 . These parameters do not provide maximum bandwidth, but has a low center frequency as needed.

5. EMI PERFORMANCE

It is known that the P/GBN can cause a significant EMI issue in high-speed circuits because of the resonance effect in the cavity formed between the power and ground planes. Low radiated emission or EMI is important in high speed circuits for the compliance of the strict EMC regulations. Here, the EMI behavior of the proposed PCPL by comparing with the reference board is numerically and experimentally investigated. The test board is put on a wooden table, and the RF signal of 0 dBm generated by the signal source (HP 8324) is launched into the power plane of the board through port1. The radiated -field from 1 to 8 GHz is measured by the horn antenna (R&S HF906). The wooden table with a test board is rotated in 360 at the speed of 4.5 /s for each excited frequency point, and the maximum radiated -field is recorded by the spectrum analyzer (R&S FSP) with 100-kHz resolution bandwidth. The radiated -field in the 3-m test distance is also modeled by HFSS. Fig. 6 (a) and (b) shows the simulated and measured EMI radiation at 3-m distance for the SL PCPL and TL PCPL board, respectively. There is approximately 35-dB EMI reduction on maximum and approximately 30-dB improvement on average within two stop bands.

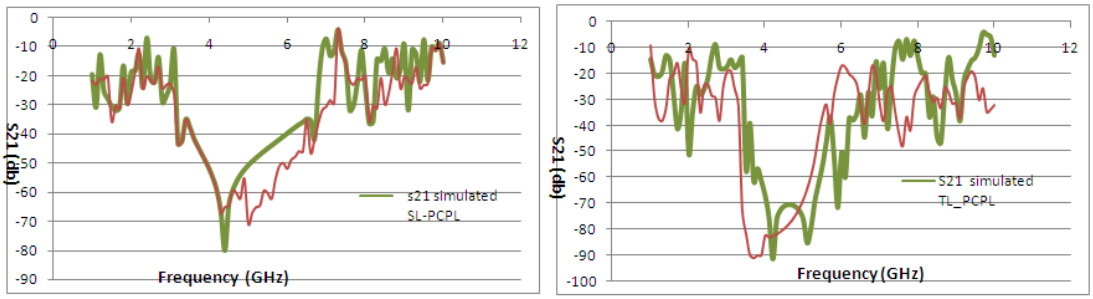

Fig. 6. Simulated and measured EMI radiation at 3 m for: (a) SL board and (b) TL board

6. CONCLUSION

A novel PCPL has been proposed to suppress the P/GBN or SSN in a high-speed circuit package. The PCPL has been fabricated by periodically embedding the high dielectric-constant material (rods) into the original isolation layer between the solid power and ground planes. Two types of PCPL lattice structures have been discussed: one is the SL PCPL and the other is the TL PCPL. It is found that both PCPLs provide excellent P/GBN elimination capability with over 60 dB on average reduction of the power noise and over totally 4-GHz

bandwidth below the 10 GHz range. In the time-domain measurement, both PCPLs can efficiently eliminate the SSN with approximately 90% reduction. In addition, the EMI caused by the P/GBN is also efficiently suppressed within the stop band with 30-dB reduction on average. All the excellent SI/PI and EMI performance are verified both by the numerical simulation and experimental measurement. Good agreement is seen.

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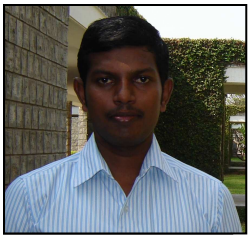

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